Long Distance Differential Transmission of DS Links over Copper Cable

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0. Introduction

The INMOS DS links [5] are characterized for transmission on 100 ohm impedance printed circuit traces for point connection on a printed circuit board over distances of up to 30 cms. INMOS recommends the use of the AT&T 41 series transceivers driving differentially over copper cable for distances up to 10 meters using a pseudo-ECL technique. Associated with this is a proposed cable specification and a termination scheme for either resistive or diode termination.

This paper examines the performance of the 41 series drivers as a function of cable length, signal frequency, bit pattern sensitivity and common mode rejection when used with traffic with DS link characteristics.

One goal of this study is to determine the relative importance and performance of the different termination options. This issue has an impact on the layout, packing density and cost of bringing DS links off printed circuit boards using this technology. Given that different vendors may make different value judgments of the preferred method we have also studied the effects of mixed resistive/diode connections.

This is the first release of the study and it has not been possible to study any possible effects due to the proposed Harting and Fujitsu connectors which have not yet been made available to us.

1. Measurement Setup

The test environment is comprised of two test boards coupled by a chosen length of cable and driven either by a high precision pulse generator or a bit error rate tester (BERT). Timing measurements were made with a 1Gigasample/sec digital oscilloscope. The architecture of the test board and the main specifications of the instrumentation are given below.

1.1. Test Board

A test board was designed to interface to existing test equipment. SMD components were used for the line transceivers and their associated termination circuitry. The placement of these components was optimized for minimum trace length, to alleviate problems with impedance mismatch.

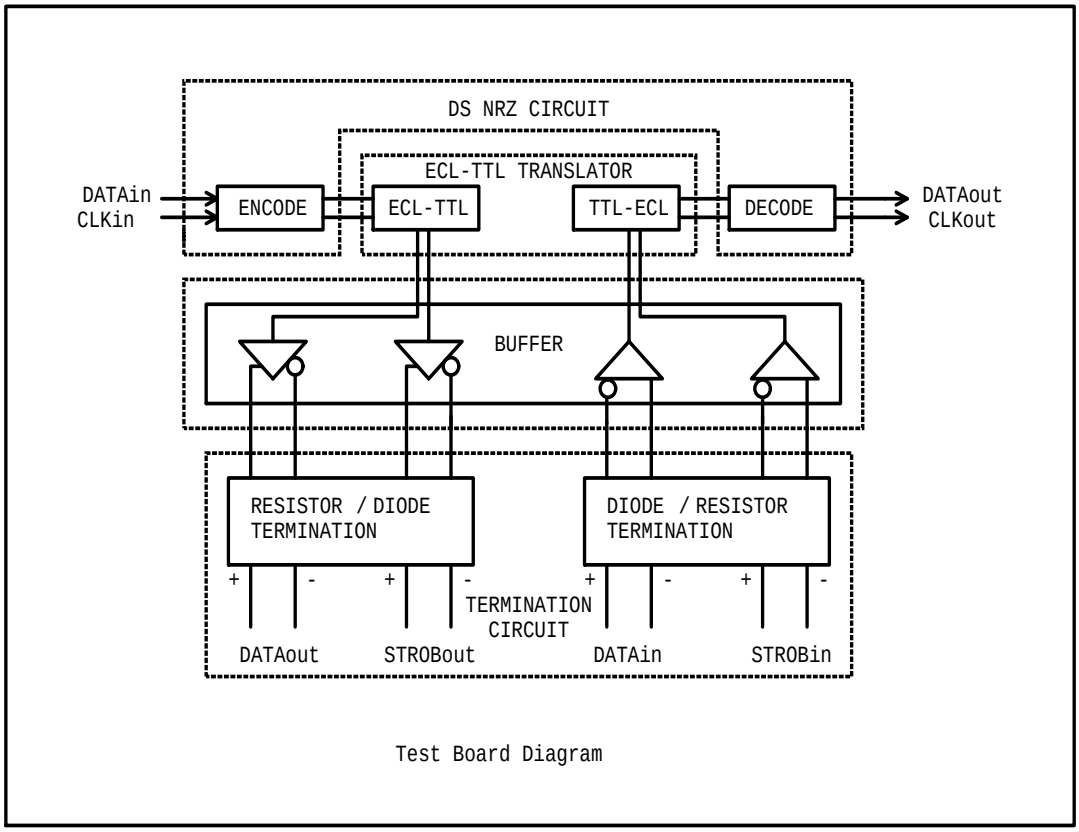

Figure 1 : Test board diagram

The test board consists of four functional blocks : the NRZ-to-DS encoder/decoder, the ECL-TTL level-translators and the AT&T differential line drivers/receivers with their associated termination circuitry. The detailed schematics of the board are included in appendix A1.

The NRZ-to-DS encoder/decoder converts the data and clock signals from the BERT to a data and strobe signal pair, which conforms to the bit level T9000 DS-link protocol. This part of the circuit is realized in ECL technology, so that it would not be the limiting factor for the transmission speed.

The ECL-TTL level translator interfaces between the ECL signals from the encoder/decoder and the TTL inputs and outputs of the AT&T buffers.

Figure 2 illustrates the signal flow when two test boards are connected in a typical measurement setup using the DS-encoder/decoder. The block labeled termination corresponds to either the diode or the resistor cable termination circuit.

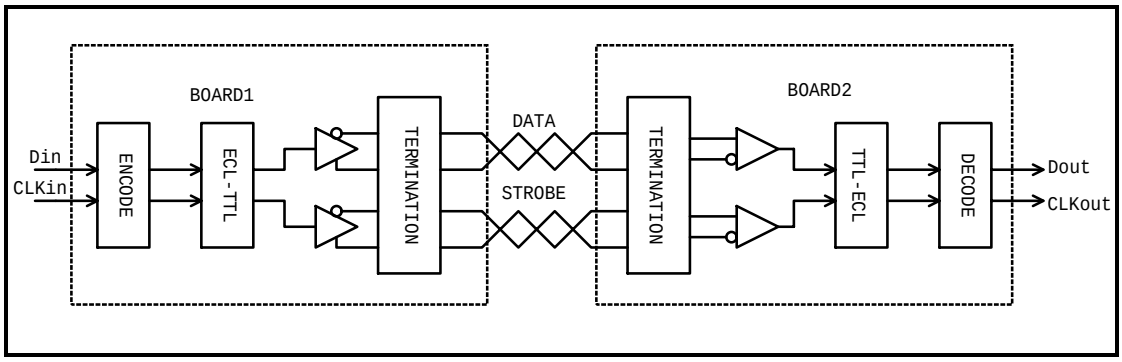

Figure 2 : Example measurement setup

1.1.1 Pseudo-ECL Line Drivers/Receivers

The 41-Series of high performance differential line drivers and receivers from AT&T are used to interface to the cable. These devices translate TTL I/O signals to pseudo-ECL (PECL) levels suitable for high-speed data transmission [1]. Pseudo-ECL levels are ECL levels shifted by 5V to run off a single power supply. The 41Mx devices are specified for 400MBits/s maximum data rate. The typical output levels of driver are shown in figure 3. The pseudo-ECL receiver input common-mode range is from -1.2v to 7.2V and is centered ±4V around the typical output of the driver.

A list of the key features of the AT&T buffer is given below :

- Very small driver output skew
- Large common mode range
- Bit rates up to 400MBit/s

On the test board the 41ML transceiver is used. This device already includes the pulldown resistors necessary for the open-emitter ouputs of the driver, thus saving some PC-board space, but increasing the power dissipation of the package by about 250mW. The complete data sheet is included in appendix A2.

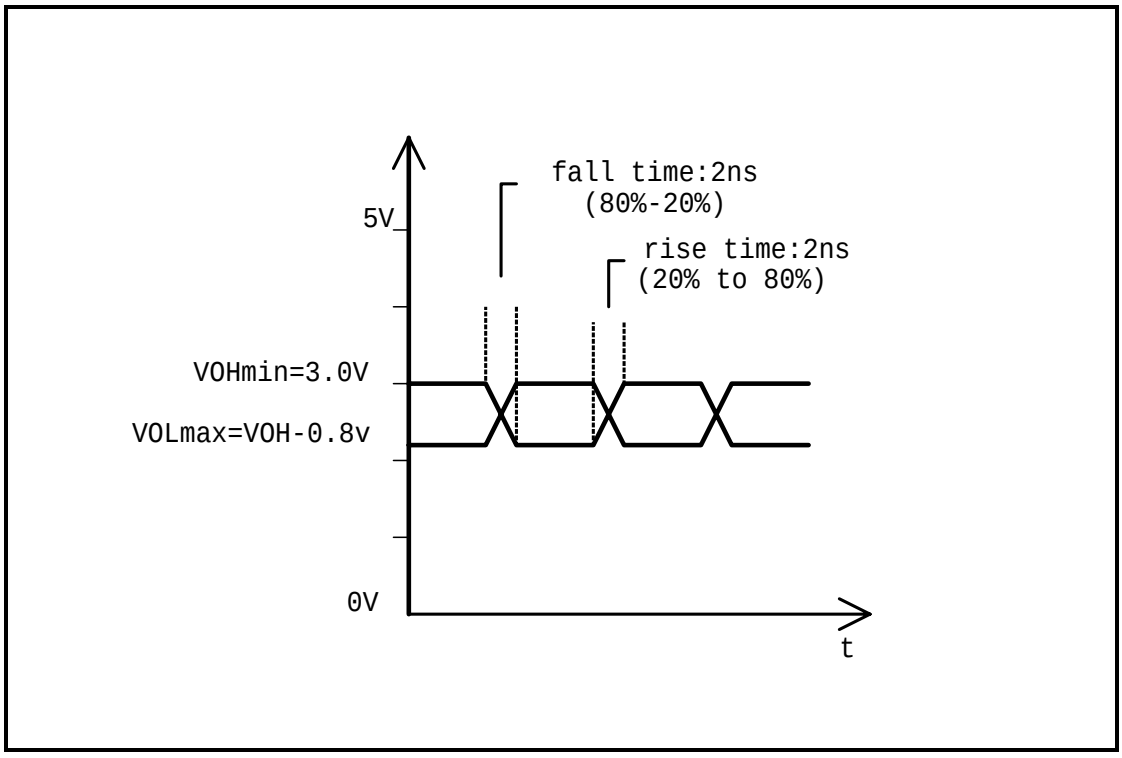

Figure 3 : Output levels of the AT&T driver

1.1.2 Cable Termination

DS links transmit at 100 Mbaud and therefore transmission line effects must be taken into account. Resistive termination is efficient only when the true impedance of the line is known and matched. Diode termination (see below) does not require such close matching and all signal overshoots are effectively clamped.
Experience gained with routing PCB's employing these techniques has shown that a high level of complexity is required to satisfy the needs for minimum trace length, maximum packing density for the front panel connectors and simple layouts for the SMD devices.
For the resistor termination circuit (R.T.), a simple split termination configuration was used [1]. The termination resistor was matched to the cable impedance (85ohms, see section 1.3). The advantages of this type of termination are :

- Simple, small component count
- PC-board space requirement is small, this leads to dense packaging and therefore short traces for the critical high speed signals

In the diode termination circuit (D.T.), schottky-diodes perform the function of the termination resistor (see [2]). The differential resistance of the diodes changes with the input voltage, so the termination adapts to the cable impedance. The diode termination circuit also includes protection diodes, which protect the inputs and outputs of the AT&T buffers from large common mode voltages. The advantages of diode termination can be summarized as follows :

- No impedance matching is required
- Overshoot, ringing and external noise is clipped by the termination diodes
- Includes protection circuitry

This termination circuit does require a considerably larger amount of PC-board space though.

1.2. Instrumentation

The following list gives an overview of the instruments used for the measurements and their respective characteristics.

Bit Error Rate Tester (BERT)

PF-5 Error Test Set, Wandel & Goltermann

- Bit rates up to 175 MBit/s
- Various pseudo-random bit sequences from $2^6 - 1$ to $2^{31} - 1$
- Detection of bit slip

Oscilloscope

TDS 540 Digitizing Oscilloscope, Tektronix

- 500 MHz maximum analog bandwidth
- 1 Gigasample/second maximum digitizing rate
- Four-channel acquisition
- Waveform math
- Eight-bit digitizers
- Up to 15,000-point record length

Pulse Generator

Pulse Generator 9210, plug-in module 9211, LeCroy

- Frequency up to 250 MHz
- adjustable rise/fall times (min. 1ns)

1.3. Cable Characteristics

The INMOS DS link standard includes the following requirements for a cable to be used for differential DS link transmission : the cable should consist of four shielded twisted pairs with an overall shield and the differential impedance of the pairs should be 100 Ohms.

The following specification applies to a suitable cable recommended by INMOS for use with buffered DS-links. This cable has been manufactured (by Madison Cable Corporation) according to specifications by INMOS :

- Cable type : Twisted pair individually shielded cable
- Conductor : AWG30
- Cable Impedance : 90 ± 9 Ω
- Linear Resistance : 350 Ω/km
- Time Delay Skew : 0.15 ns/m
- Attenuation(Differential) : 450 dB/km (Maximum @ 50MHz)
- Near End Crosstalk (backward) : 2% Max. (50 MHz @ 10 Meter cable)
- Far End Crosstalk (forward) : 4% Max. (50MHz @10 Meter cable)

Due to difficulties with procurement of the INMOS cable, we selected a similar cable manufactured by Cables Pirelli which was readily available at CERN and also conforms to the mechanical (outer diameter) and electrical requirements (cable impedance, attenuation) of differential DS-link signal transmission. Another objective was to find out if a cable without individually shielded pairs could be used without a loss of performance. The main specifications of this cable are given below :

- Cable type : Twisted pair multiconductor shielded cable
- Conductor : AWG26
- Cable Impedance (typical) : 85 Ω
- Linear Resistance : 150Ω/km
- Cable Capacitance : 80 nF/km
- Attenuation
  - at 1 MHz : 34 dB/km
  - at 10 MHz : 113 dB/km
  - at 50 MHz : 253dB/km
- Crosstalk (at 1 MHz) : 55 dB/500m

The overall characteristics of the two cable types are similar, but the Pirelli cable uses a thicker wire. This is possible at the same cable diameter, because the space for the individual shields is saved compared to the Madison cable. Therefore the attenuation and the linear resistance of the Pirelli cable are somewhat better. The other main difference is crosstalk. Although it is difficult to compare the given data (because it applies to different frequencies), it can be expected that the individually shielded version should provide lower crosstalk levels (if one assumes that crosstalk scales linearly with cable length, the crosstalk for a 10m cable would be 21dB or 9%).

1.4. Environmental conditions

Measurement Environment:	Laboratory Environment
Temperature:	Room temperature
Supply Voltages:	V_{CC} = +5V
	V_{EE} = -5.2V

2. Measurement Results

In the following sections the main factors that limit transmission speed and cable length are treated (sections 2.1 to 2.3). The results for the maximum transmission speed are presented in section 2.4. Finally in section 2.6 the effects of common mode voltage (e.g. different ground levels) are studied.

2.1. Amplitude Measurement

The attenuation of the cable will reduce the amplitude of the differential signal at the receiver input. When the receiver input signal is smaller than the input threshold, the transmission will fail. To obtain a reliable communication channel (low error rates), a margin has to be added, to allow for noise, crosstalk, EMI and other disturbances. As cable attenuation is a function of cable length and signal frequency, this should put an upper limit on transmission speed and distance.
Cable attenuation can be considered to increase linearly with cable length, while attenuation per unit-length is approximately proportional to the square root of frequency (due to the skin-effect loss) in the frequency range of interest here :

$$A = k \cdot \sqrt{f} \cdot l$$

where, A is the attenuation in dB, f is the signal frequency in MHz and l is the cable length in km.
Because the linear resistance of the selected cable is only 0.15 Ω/m, it may be safely ignored with respect to the cable characteristic impedance (for a cable shorter than 30 meters, the linear resistance is smaller than 4.5 ohms).
From the parameters given in the cable specification (see section 1.3), we can derive the constant k for the selected cable as :

$$k = -35.7 \qquad [\mathrm{dB} / (\mathrm{km} \cdot \sqrt{\mathrm{Hz}})]$$

The cable attenuation can also be also defined as:

$$A = 20 \cdot \log(V_{receiver}/V_{driver}) \qquad [\mathrm{dB}]$$

where, $V_{receiver}$ is the peak-to-peak differential input voltage at the receiver and V_{driver} is the peak-to-peak differential output voltage at driver end. Therefore :

$$V_{receiver} = V_{driver} \cdot 10^{\frac{1}{20} \cdot A} \cdot \quad [\mathrm{V}]$$

If we know the output voltage of the driver, we can now calculate the expected input voltage at the receiver using the above equations. It has to be noted though, that the attenuation as given above is defined only for sine wave signals and for lines properly terminated with a resistive load matching the cable characteristic impedance.

2.1.1. Amplitude versus cable length

Setup

Figure 4 shows the measurement setup. The differential PECL-signal was measured on the driver and receiver end of the cable (for diode and for resistor termination). The measurement was carried out with different length of cable. The input signal was a 50 MHz continuous square wave signal with 50% duty cycle from the pulse generator. This corresponds to an alternating sequence of zero and one bits at 100MBit/s, which is the nominal transmission speed for DS-links.

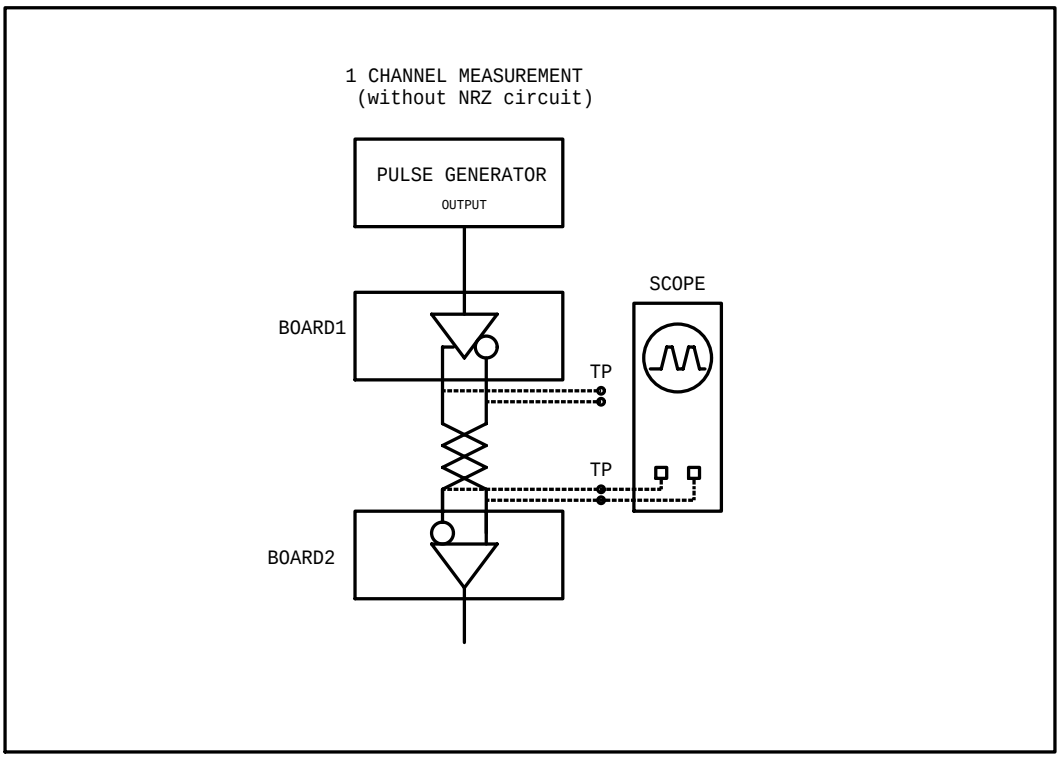

Figure 4 : Measurement setup

Results

Table 1 shows the measurement results. A graphical representation of the results is given in figure 5 (see below). By measurement, we determined the differential output voltages of the driver as V_{driver} = 1.25V for diode termination and V_{driver} = 2.5V for resistor termination.

Cable Length [meter]	Amplitude[V_{pk-pk}]					
	Diode Termination			Resistor Termination		
	Measured Data	VMI	Theoretic Data	Measured Data	VMI	Theoretic Data
1	1.00	0.60	1.21	2.50	2.10	2.43
10	0.95	0.55	0.95	2.10	1.90	1.90
15	0.90	0.50	0.83	1.50	1.10	1.65
30	0.80	0.40	0.55	1.00	0.60	1.10

Table 1 : Receiver differential input voltage vs. cable length

As stated in the electrical characteristics (see appendix A2), the minimum peak-to-peak differential input voltage of the receiver must be larger than 0.4V. So we can define the input noise margin (VMI) as :

$$VMI = VAR_{msr} - DIV_{min} \quad [V_{pk-pk}]$$

$$DIV_{min} = 0.4V$$

where VAR_{msr} is the measured peak-to-peak receiver differential input voltage and DIV_{min} is the minimum receiver differential input signal (DIV_{min} = 2 V_{th} , V_{th} = 0.2V from the specifications, see appendix A2).

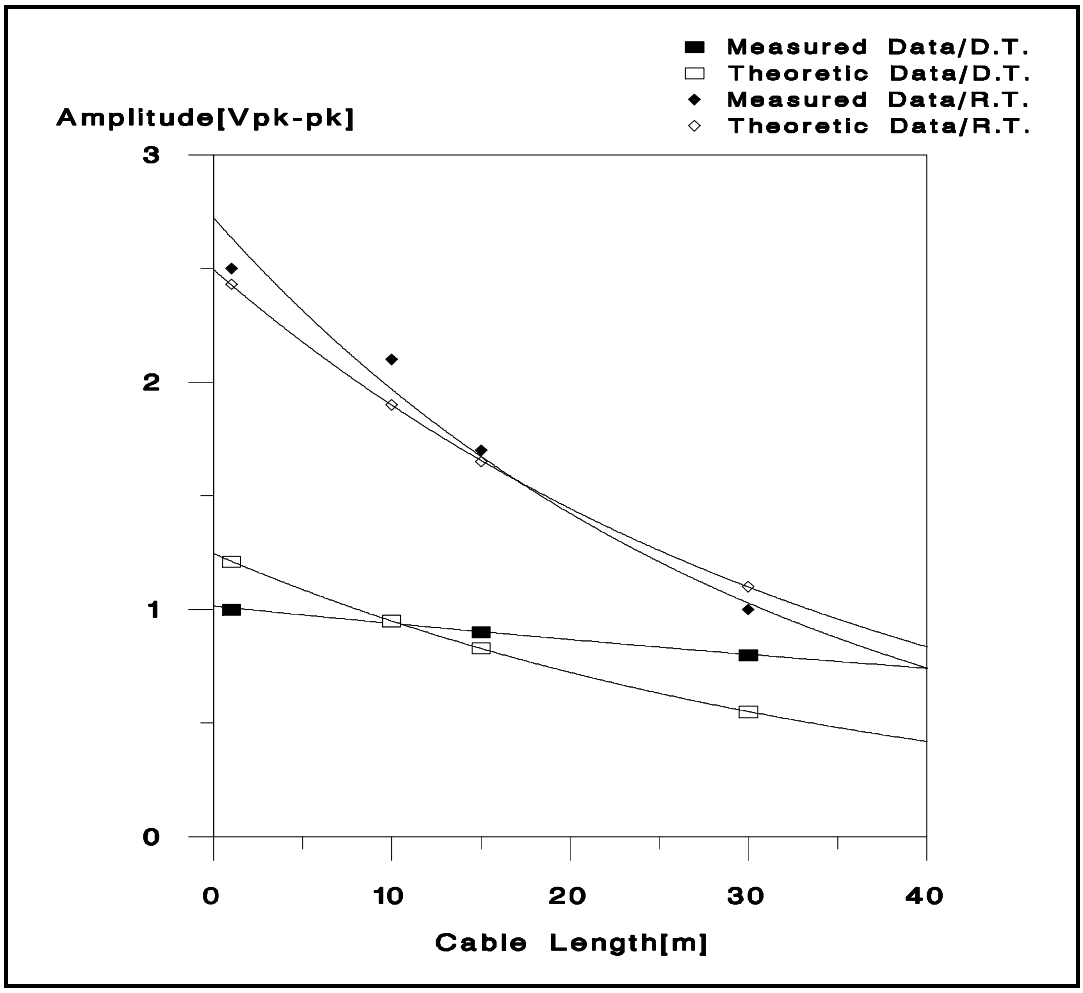

Figure 5 : Receiver differential input voltage vs. cable length

Conclusions

All the results show a very good input noise margin, even for a 30 meter cable. On the other hand, disturbances like crosstalk and EMI will tend to decrease this margin.
It is also obvious that the differential input signal of the resistor terminated receiver is larger than for the diode termination, resulting in a smaller noise margin for diode termination. This reduction of the signal amplitude is due to the clamping function of the termination diodes (see section 1.1.2).
From figure 5 it can be seen that the measured data and the theoretical data match very well for resistor termination. For diode termination, the slope of the measured and the calculated curve is different. The reason for this discrepancy is that the theoretical relationship used is only valid for a transmission line with resistive impedance matching termination (see above). The occurrence of reflections also tends to influence the measurement results.

2.1.2. Amplitude vs. frequency

Setup

The setup is the same as in figure 4. A 10 meter cable is used here for all measurements. The frequency of the square wave input signal is changed. The measured frequencies correspond to bit rates of 25, 50, 100 and 150MBit/s respectively.

Results

The measurement results are shown in table 2, with a graphical representation in figure 6

Signal Frequency [MHz]	Amplitude[V_{pk-pk}]			
	Diode Termination		Resistor Termination	
	Measured Data	Theoretical Data	Measured Data	Theoretical Data
12.5	1.08	1.09	2.40	2.18
25.0	1.06	1.03	2.20	2.05
50.0	0.93	0.95	2.10	1.90
72.5	0.80	0.89	2.0	1.78

Table 2 : Receiver differential input voltage vs. frequency

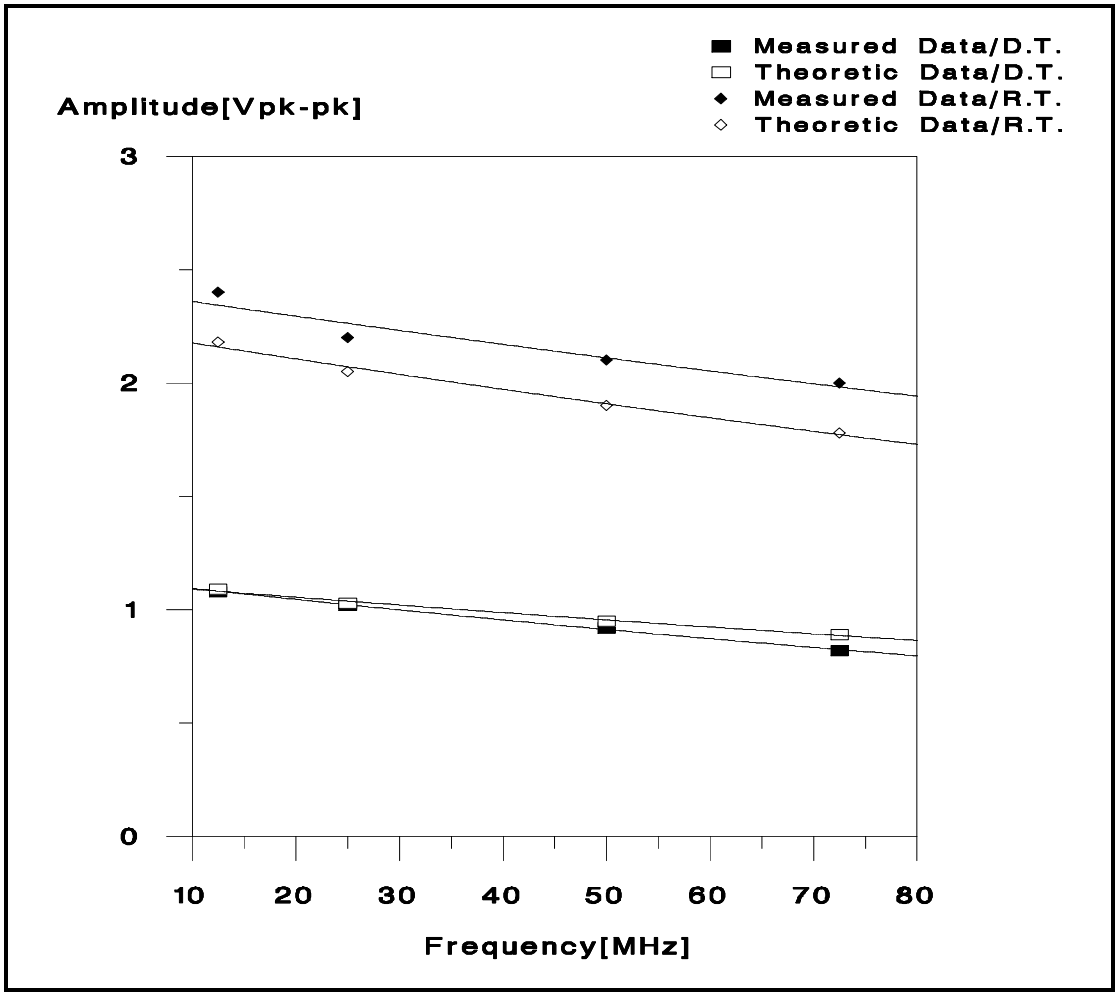

Figure 6 : Receiver differential input voltage vs. frequency

Conclusions

From table 2, the worst-case receiver input signal for diode termination is 0.8V, measured at 72.5MHz, which is equivalent to a bit rate of 150MBit/s. This still leaves a margin of 0.4V or 50% of the input signal swing. For resistor termination the margin is even 1.6V or 80% of the input signal.
It is important to note though, that the reduction of the received input signal is not the only effect that will limit the transmission speed. Other limitations like jitter and skew will be discussed further on.

2.1.3. Eye Diagram Measurement

The previous measurements do not reveal pattern dependent effects, due to the regular nature of the test signal. Therefore the eye-diagram at the receiver input was measured as described below.

Setup

The measurement setup is similar to the setup used in section 2.1.1 (see figure 4). For this measurement the BERT is used instead of the pulse generator to generate the input signal to the driver. The test pattern is a long pseudo-random sequence (pattern PRS31, see also section 2.4.1). The eye-diagram is measured using the scope in infinite persistence display mode. The trigger signal comes from the bit clock output of the BERT. All measurements are performed at 100MBit/s.

Results

The results in table 3 show the vertical eye-opening of the differential receiver input voltage. The eye-opening was measured in the middle of the bit window. The table also includes the input noise margin (VMI, see also section 2.1.1).

Cable Length [meter]	Amplitude[V_{pk-pk}]			
	Diode Termination		Resistor Termination	
	Measured Data	VMI	Measured Data	VMI
1	0.94	0.54	2.10	1.70
10	0.90	0.50	1.70	1.30
15	0.80	0.40	1.40	1.00
30	0.40	0.00	0.50	0.10

Table 3 : Receiver differential input eye-opening vs. cable length

Figure 7 shows a hardcopy of the receiver input eye-diagram for a 10 meter cable with resistor termination.

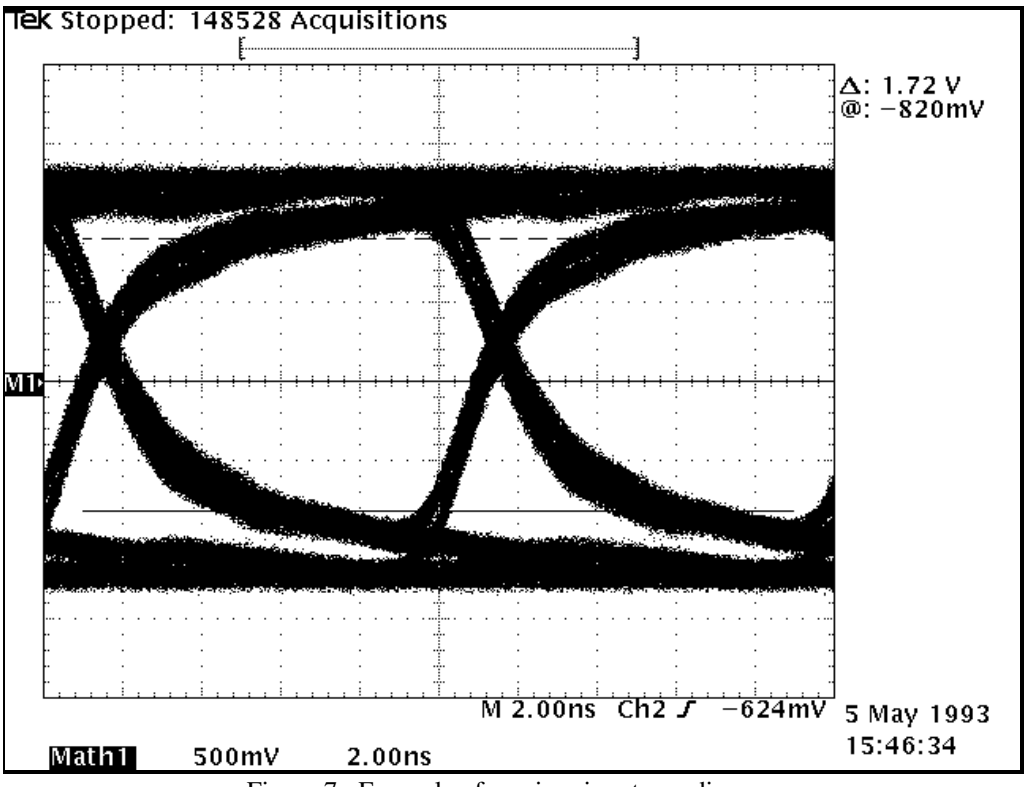

Figure 7 : Example of receiver input eye-diagram

Conclusions

The results in table 3 show that for the 30 meter cable there is no noise margin for the diode terminated receiver and a very small margin of 0.1V for the resistor terminated transceiver. This means that reliable transmission at 100MBit/s over 30 meters is not possible with the selected cable and transceiver circuits.
The eye-opening for the resistor termination is much larger than for the diode termination. This is due to the clipping action of the termination diodes (see 2.1.1).
Comparing the results from table 1 (receiver differential input voltage with square wave input signal) and table 3, one finds that the useful input signal amplitude is smaller for the random pattern, especially for the 30 meter cable. This is due to the lowpass characteristics of the cable, which will reduce the effective eye-opening. A longer cable will have a lower cutoff frequency. Therefore the difference between the measurements is particularly marked for the 30 meter cable.

2.2. Crosstalk Measurement

Crosstalk is due to capacitive and inductive coupling of signals between parallel lines. It can decrease the effective amplitude of the useful signal and generate additional jitter.
We have to consider both near-end and far-end crosstalk, though near-end crosstalk is expected to be the dominant effect in our application.

Setup

The figures 8 and 9 show the measurement setup. For the first measurement, only one channel is active, and the near-end and far-end crosstalk signal can be measured at the receiver input on the respective ends of the cable (see figure 8).
For the second measurement, two channels are active, with signal flow in both directions. In this case of bi-directional transmission, the effects of near-end and far-end crosstalk overlap and cannot be measured independently (see figure 9).
The input signal for these tests is a 50MHz continuous square wave (duty-cycle of 50%), which is equivalent to a bit rate of 100MBit/s. The input of the channel on which crosstalk is measured is connected to ground.

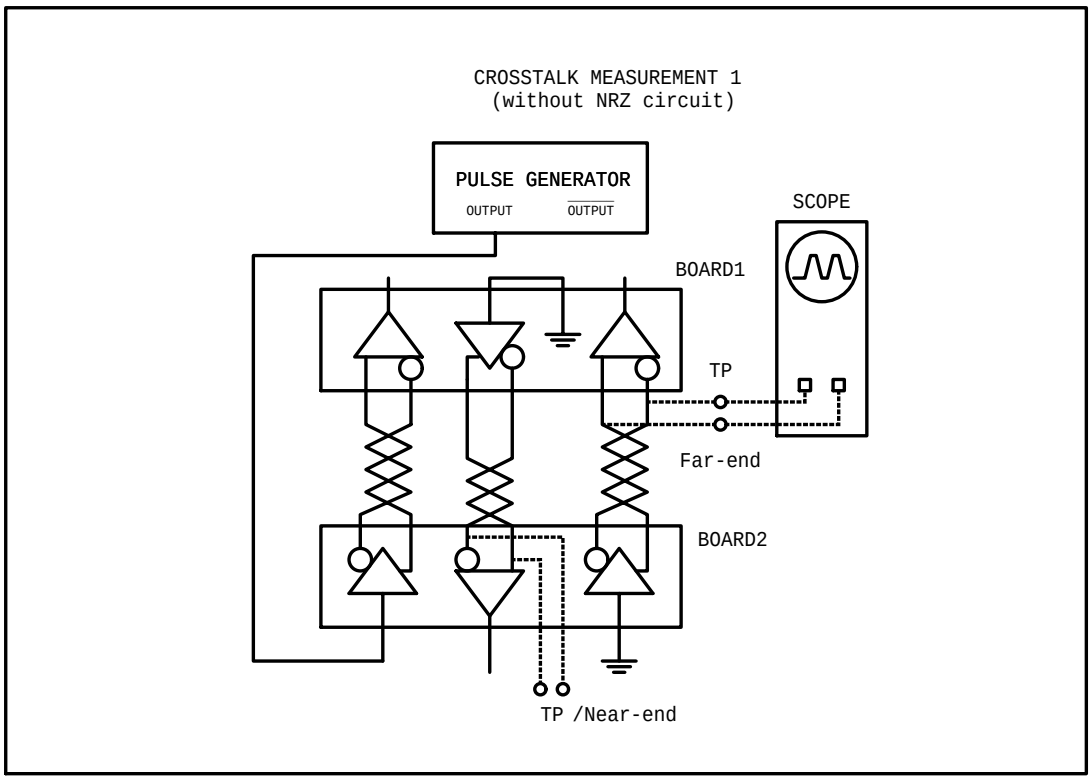

Figure 8 : Crosstalk measurement with one active channel

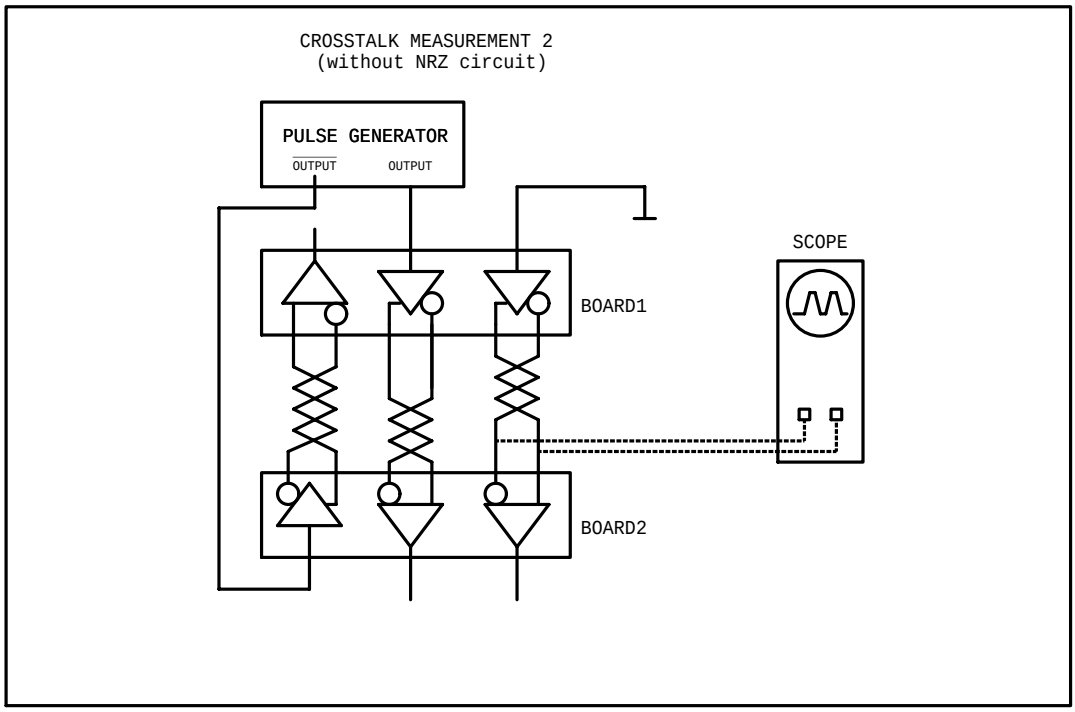

Figure 9 : Crosstalk Measurement with two active channels

Results

Data in table 4, 5 and 6 show the peak-to-peak values of the crosstalk on the receiver differential input of a quiet channel.

Cable Length	Diode Termination		Resistor Termination	
[meter]	Crosstalk[mV]	VM[mV]	Crosstalk[mV]	VM[mV]
1	100	400	90	1720
10	60	430	50	1600
15	90	320	80	940
30	100	200	90	420

Table 4 : Near-end crosstalk measurement, one active channel

Cable Length	Diode Termination		Resistor Termination	
[meter]	Crosstalk[mV]	VM[mV]	Crosstalk[mV]	VM[mV]
1	70	470	130	1840
10	40	470	90	1720
15	40	430	70	970
30	30	340	40	520

Table 5 : Far-end crosstalk measurement, one active channel

Cable Length	Diode Termination		Resistor Termination	
[meter]	Crosstalk[mV]	VM[mV]	Crosstalk[mV]	VM[mV]
1	190	220	170	1660
10	150	250	90	1520
15	150	200	90	920
30	170	160	110	380

Table 6 : Crosstalk measurement, two active channels

VM is the resultant margin of the receiver input voltage. It is calculated as :

$$VM=VMI-2\cdot Crosstalk$$

where, VMI is the input noise margin obtained from the amplitude versus cable length measurement (see section 2.1.1).

Conclusions

The results from table 4 and 5 show that the values for near-end and far-end crosstalk are similar for short cables, but far-end crosstalk is reduced with cable lenght, while near-end crosstalk stays approximately constant.
Comparing table 4 and 5 with table 6, it can be seen that crosstalk is approximately doubled when two channels are active.
From table 6, the minimum input noise margin for diode termination with a 30 meter cable is 160mV. This is similar to the noise margin of standard ECL logic (for 10kH the worst case noise margin is 150mV) For resistor termination with a 30 meter cable, the margin is much larger with 380mV.

2.3. Jitter and Skew Measurement

Jitter is the deviation of the signal transitions from their nominal position in time. This will cause a timing uncertainty when sampling the data with the clock recovered from the DS-signal. Jitter therefore tends to increase the error probability and excessive amounts of jitter will eventually cause the transmission system to fail.
We consider two types of skew here, first the duty cycle skew of an individual signal, and second the skew between a DS-signal pair.
From the AC-characteristics of the T9000 the minimum input edge resolution of the DS-link input is known to be t_{LIHL} = 2ns (see figure 10).

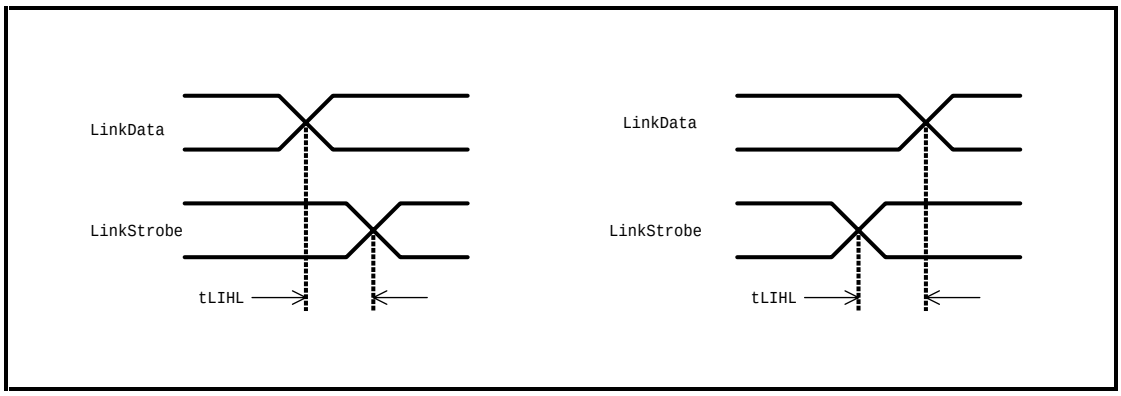

Figure 10 : DS input edge resolution

Assuming the target bit rate of 100MBit/s, the time margin on the input edge resolution can therefore be defined as :

$$Mj = T - J_{pk} - t_{LIHL} - \Delta t_{DSO} = 7\text{ns} - J_{pk}$$

where T is the bit period (T=10ns here) and J_{pk} is the maximum peak-to-peak jitter, including duty-cycle skew and signal skew. Δt_{DSO} is Data/Strobe output skew (maximum is 1 ns). This is illustrated below in figure 11.

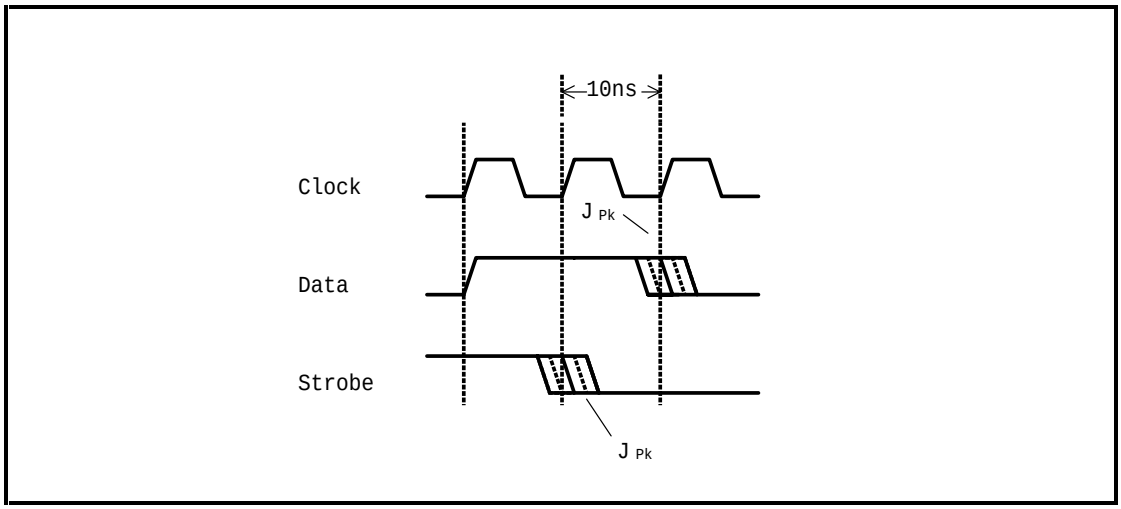

Figure 11 : DS input timing margin

2.3.1. Duty Cycle Skew Measurement

Duty cycle skew, also called duty cycle distortion or pulse width distortion, is defined as the deviation of the bit period from its nominal value. This is mainly caused by the difference in propagation delays for low-to-high and high-to-low transitions. In our application this can essentially be attributed to the line drivers and receivers, as the cable is supposed to behave as a linear system.

Setup

The input signal for the duty cycle distortion measurement is a 50 MHz continuous square wave. The duty cycle is 50%. In order to find out whether the signal duty cycle skew will increase when more than one channel is active, the measurement is divided into two steps, one channel and two channels measurements. See figure 12 and figure 13.

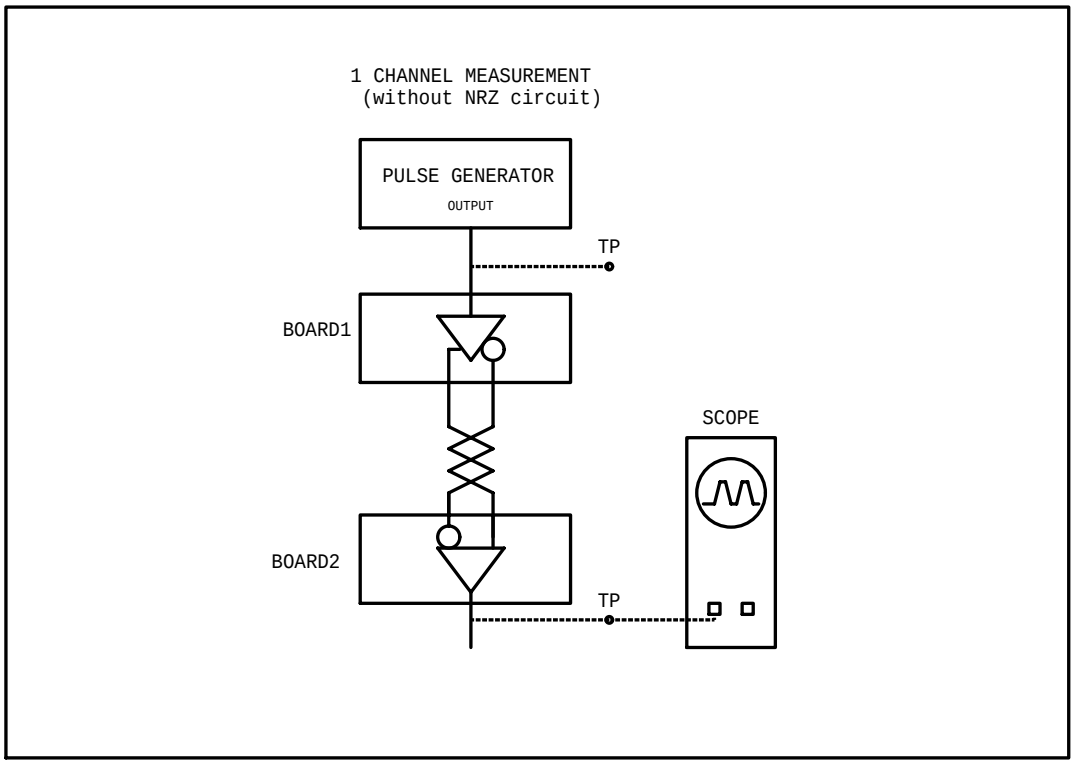

Figure 12 : Duty cycle skew measurement setup with one active channel

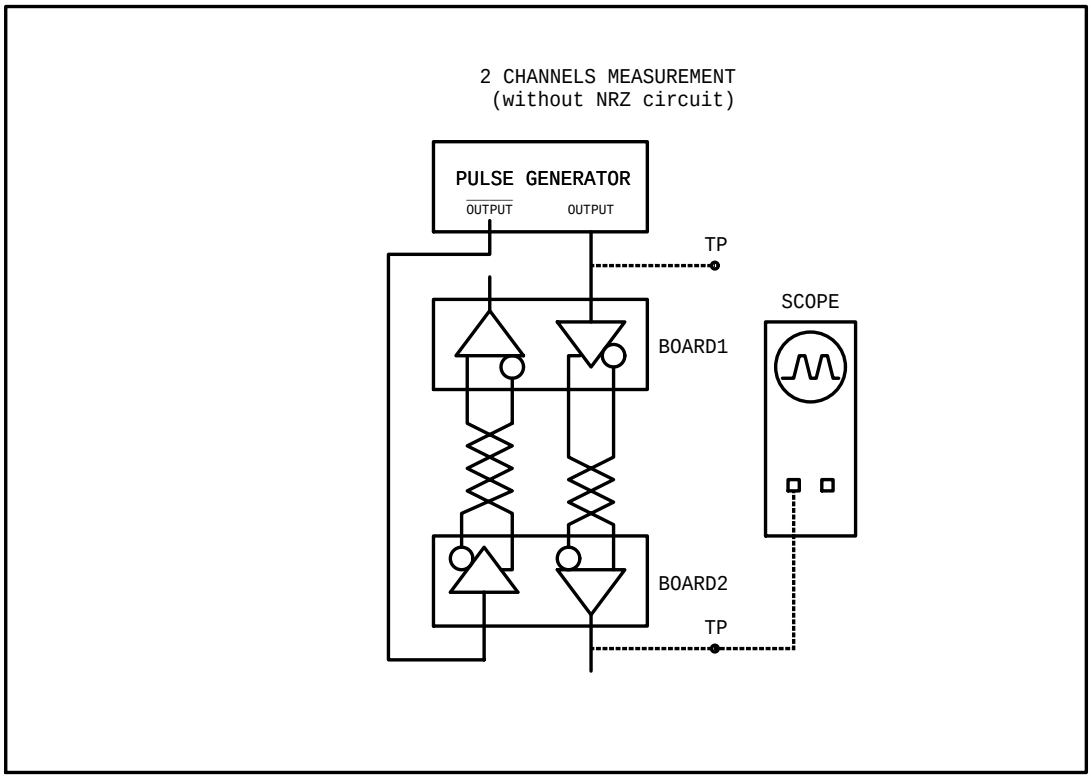

Figure 13 : Duty cycle skew measurement setup with two active channels

Results

Table 7 shows the results of the duty cycle measurement.

Cable Length [meter]	1 Channel Duty Cycle Skew[ns]		2 Channel Duty Cycle Skew[ns]	
	D. T.	R. T.	D. T.	R. T.
1	0	0	0	0.4
10	0.3	0.3	0	0
15	0.3	0.3	0.4	0.5
30	1.1	0.7	1.5	1.2

Table 7 : Duty cycle measurement of 41ML receiver output

All the skew values for cable length up to 15 meters are very small and can be neglected. The duty cycle skew for the 30 meter cable is less than 1.5ns, only slightly reducing the input timing margin. The values measured for diode termination and resistor termination are nearly the same.
Comparing the results for the one channel and the two channels measurement, one can see that the difference of duty cycle skew is very small, though there is more noise on the signals for the two channel measurement (see the waveforms in appendix A3)

Conclusions

The measured values of duty cycle distortion are small compared to the nominal bit period of 10ns (i.e. worst case 15% of the bit period for diode-termination, two channels).
The diode termination circuit does not seem to introduce any additional duty cycle distortion.
Crosstalk does not have a big impact on duty cycle distortion with this setup. This might be different for example with other patterns.

2.3.2. DS-Signal Skew Measurement

The data and strobe signals will undergo different delays when transmitted over a longer length of cable. Excessive amounts of DS-signal skew will eventually cause the link to fail (see section 2.3). The main source of skew for long distance connections will probably be different delays of the twisted pairs in the cable, as the skew between two AT&T drivers in one package is very small ($\Delta t_{SKEW} < 0.3$ns, see [1]).
Future implementations of the DS-link module in the T9000 are supposed to include a skew correction system, which will automatically compensate skew between D and S by sending data alignment tokens [4]. This is not yet functional on the early revisions of the T9000 or the INMOS Link Test Chip (LTC) (see section 2.4.2).

Setup

The pattern chosen for the DS-signal skew measurement is a continuous sequence of two zero bits followed by two one bits. This corresponds to a square wave signal of one 1/4 of the bit rate (i.e. 25MHz at 100MBit/s). Figure 14 illustrates the resulting data and strobe signals. The signal on D and S is the same, only shifted by one bit period. This allows it to easily measure the skew between the signals.

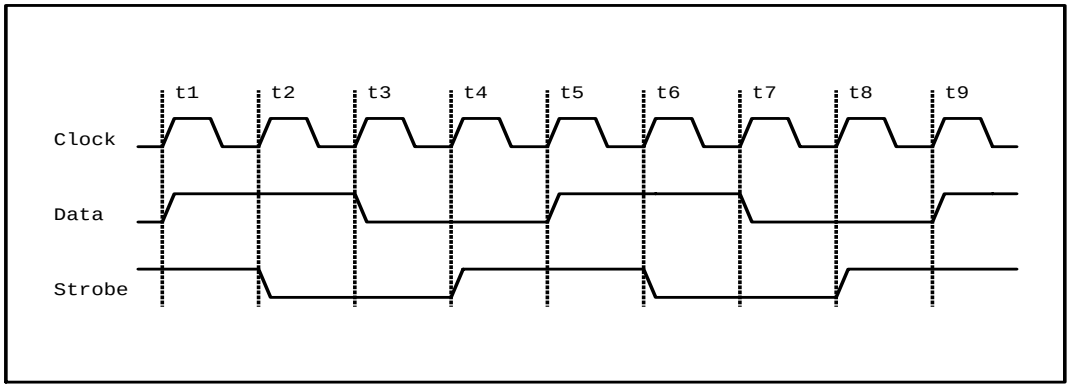

Figure 14 : Data and strobe signal for DS-signal skew mesurement

Figure 15 (see below) shows the measurement setup. For this measurement the BERT was used to generate the test pattern (the pattern was set to 00110011) and the DS-encoder/decoder circuit was enabled.

Results

In the following tables, T1 is the delay between of the rising edges on data and strobe, while T2 is the delay between the falling edges on the respective signals. The skew is measured at the TTL output of the receiver as well as on the TTL input of the driver, in order to check the skew introduced by the NRZ-to-DS encoder and the TTL-ECL level translators (see figure 15).

Cable length	D.T.		R.T.	
[meter]	T1 [ns]	T2 [ns]	T1 [ns]	T2 [ns]
1	9.6	10.0	10.2	10.2
10	9.8	10.0	9.7	10.0
15	9.6	10.0	10.0	10.0
30	9.6	10.0	10.1	10.3

Table 8 : Delay between edges of data and strobe at the driver input

Cable length	D.T.		R.T.	
[meter]	T1 [ns]	T2 [ns]	T1 [ns]	T2 [ns]
1	9.7	10.3	10.2	10.0
10	9.4	10.0	9.6	10.0
15	9.3	9.7	9.7	9.8
30	8.9	9.1	10.2	9.5

Table 9 : Delay between edges of data and strobe at the receiver ouput

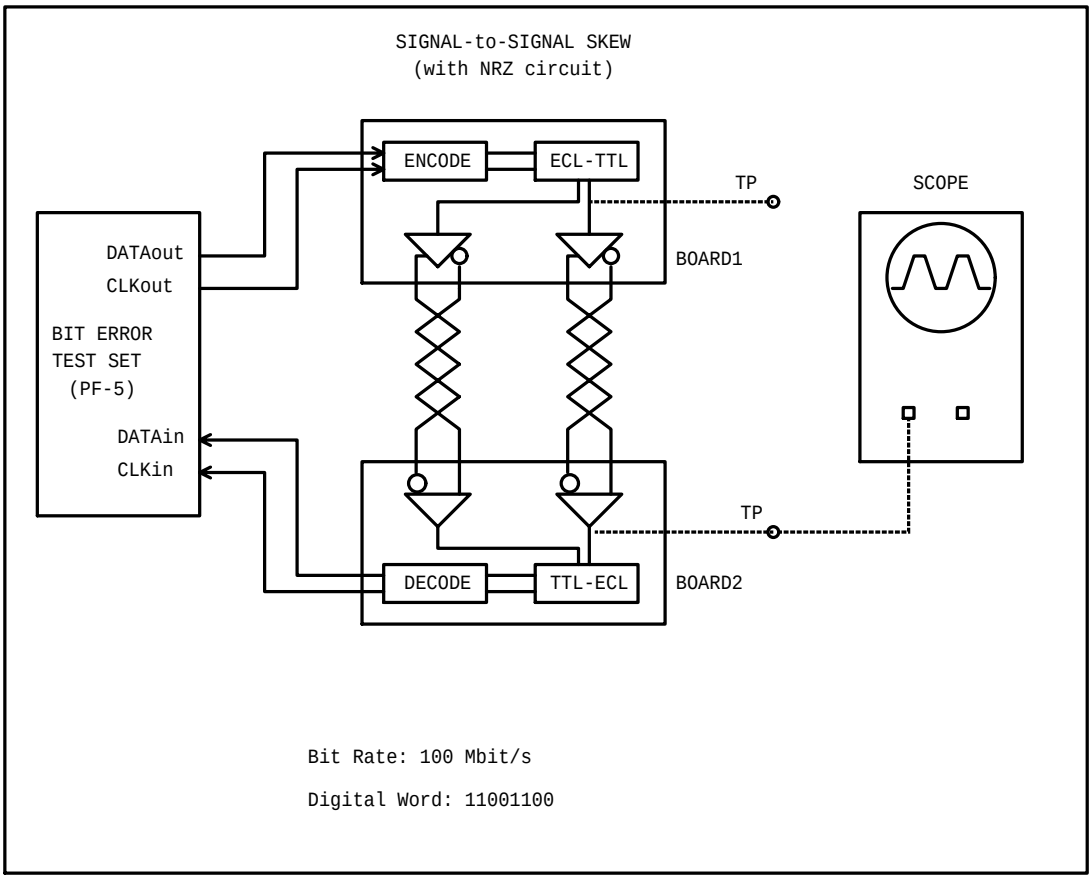

Figure 15 : Signal-to-signal Skew Measurement

Conclusions

The data measured at the driver end shows that the skew introduced by the encoding circuit and the ECL-TTL conversion is small (see table 8).
All the signal-to-signal skew values from table 9 are also quite small. The maximum of signal-to-signal skew is 0.9 ns (for diode termination with a 30 meter cable).
Therefore we obtain the overall skew as :

$$S_{pk} = S_{dcd,max} - S_{ds,max} = 1.5ns + 0.9ns = 2.4ns$$

where $S_{ds,max}$ is the maximum signal-to-signal skew and $S_{dcd,max}$ is the maximum duty-cycle skew from section 2.3.1. According to section 2.3 the resulting time margin on the input edge resolution is then :

$$M_j = 7ns - S_{pk} = 4.6ns$$

This is a margin of 46% percent of the bit window at 100MBit/s.

2.3.3. DS-Signal Jitter Measurement

The above measurements use regular patterns to determine duty-cycle distortion and signal-to-signal skew. These test signals do not reveal pattern dependent effects like data-dependant jitter (DDJ), which will reduce the effective eye-opening. Therefore jitter is measured with a pseudo-random pattern using the eye-diagram method as described below.

Setup

The setup is the same as in section 2.3.2 (see figure 15). The test pattern used is a long pseudo-random sequence (PRS31, see also section 2.4.1). The eye-diagram of the receiver TTL output signal is measured using the scope (see also 2.1.3).

Results

Table 10 shows the maximum peak-to-peak jitter measured at the receiver TTL-output. The jitter was measured at the TTL threshold (1.5V). The bit rate for all the measurement is 100MBit/s. The table also includes the time-domain eye-opening, expressed in percent of the total bit period (10 ns at 100MBit/s).

Cable length	Diode	Termination	Resistor	Termination
[meter]	J_{pk-pk}[ns]	Eye-opening[%]	J_{pk-pk}[ns]	Eye-opening[%]
1	1.2	88	0.6	94
10	1.9	81	1.0	90
15	3.1	69	1.2	88
30	---	---	6.0	40

Table 10 : Receiver output jitter

Figure 16 shows the eye-diagram for the resistor termination case, measured at the receiver TTL output, with a 10 meter cable at 100MBit/s.

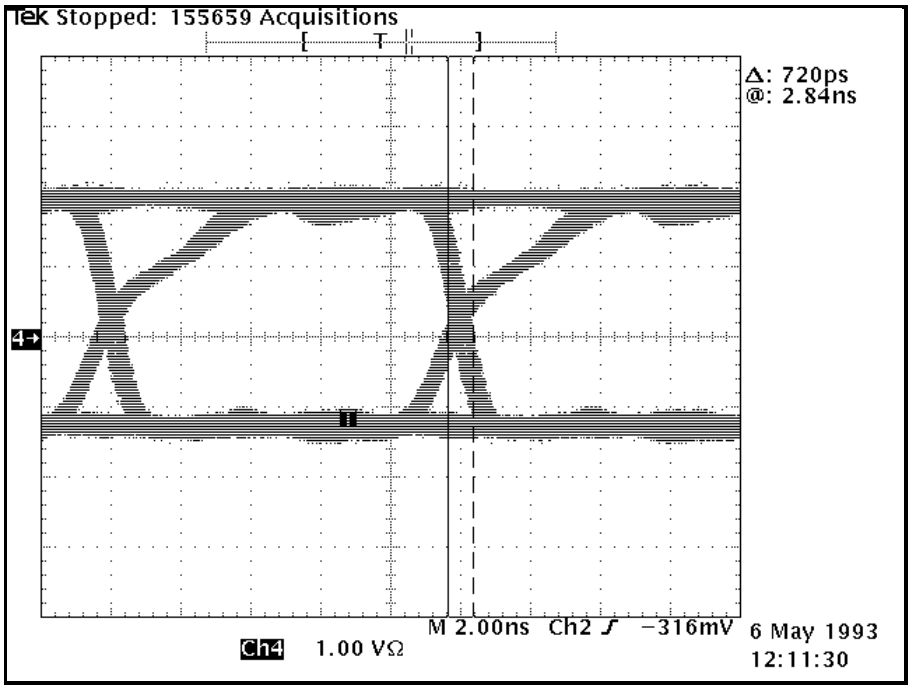

Figure 16 : Example receiver output eye-diagram

Conclusions

When judging the results, it has to be noted, that the method for measuring the eye-diagram with the scope will not display events (i.e. bit errors) occurring with a probability lower than 10^{-6}. This means that the actual peak-to-peak jitter is larger and that a timing margin has to be included for reliable communication.
For the 30 meter cable and diode termination the eye is already completely closed. The jitter for the resistor termination is also to large to allow for an input time margin (see section 2.3) taking the DS-signal skew into account. This confirms the results from section 2.1.3.
For shorter cable length, the time-domain eye-opening is much larger and should allow for secure communication.
The jitter for the diode terminated receiver is approximately two times as big as for the resistor termination.
The main jitter component here is data-dependent jitter (as random-jitter and duty-cycle-distortion are small, see section 2.3.1). In our application DDJ is mainly caused by the lowpass characteristics of the cable and the transceivers.

2.4. Speed Limitation Measurement

The purpose of this test is to determine the upper limit of the transmission speed. We therefore measure the bit rate at which the first bit errors occur immediately. We call this the speed limitation of the transmission system.

2.4.1. Measurement with the BERT

Setup

The setup is shown in figure 17. The bit error rate tester generates a serial bit pattern, which is encoded into data and strobe signals and sent down the cable. At the receiver end the DS-signal is decoded to an NRZ-serial bit stream and the clock is regenerated. The received bit stream is checked for bit errors by the BERT. The signals at the input and the output of the AT&T buffers conforms to the lowest-level (bit level) of the DS-protocol hierarchy.

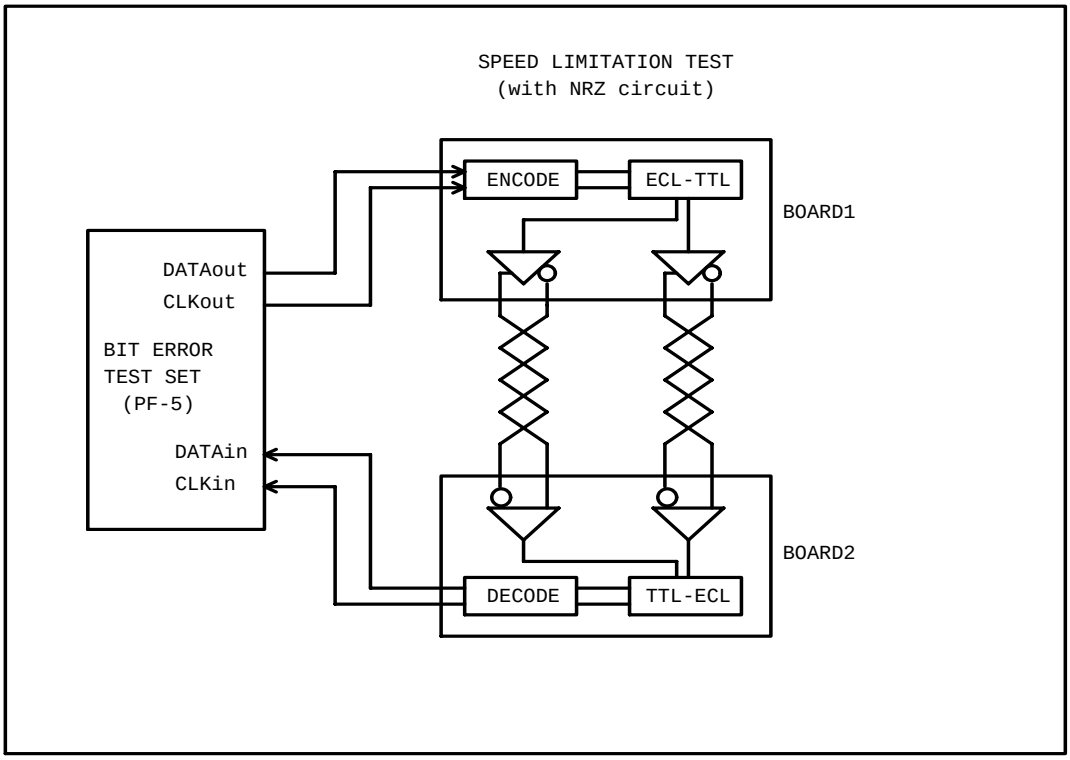

Figure 17 : Speed Limitation Measurement

The measurement procedure is as follows : The bit rate is set to 100MBit/s and then increased or decreased in steps of 500kBit/s until the first error occurs.
This test was carried out for different length of cable and with different patterns. The BERT can generate programmable patterns up to 32 bits long and various pseudo-random patterns. The following patterns were used :

- Pattern DW1: 10101010
  The first pattern is a continuos sequence of zero's and one's. This patterns contains the highest frequency components. We chose this pattern to see the effects of high frequency rolloff of the channel transfer characteristic. Skew will not affect this patterns, as the strobe signal is idle.
- Pattern DW2: 11001100
  The data and strobe signals will change state alternatively (see also section 2.3.2). Therefore this pattern will reveal the influence of mutual crosstalk between data and strobe and also limitations due to DS signal skew.

- Pattern PRS31: Pseudo-random sequence
  This is the longest random pattern of BERT ($2^{31}-1$ bits, with a maximum runlength of 31). It is expected that this pattern should contain some segments which will result in worst conditions.

It has to be noted, that none of the patterns conform to the T9000 token level protocol. Normal DS-link traffic will therefore have slightly different frequency characteristics, but the above patterns, especially PRS31 are expected to yield worst case results.

Results

The test results for different cable length, different patterns and the two termination types are presented in table 11. Some results are marked with 'no error', this means that the maximum bit rate of the BERT was reached before an error occurred. Therefore the actual value of the speed limitation is higher. A graphical representation of the data for the PRS31 pattern is shown in figure 18.

Cable Length [meter]		Speed Limitation/Diode Termination[kBit/s]	Speed Limitation/Resistor Termination[kBit/s]
1	DW1	175.0 (no error)	175.0 (no error)
	DW2	175.0 (no error)	172.5
	PRS31	170.5	169.0
10	DW1	175.0 (no error)	175.0 (no error)
	DW2	171.5	174.5
	PRS31	149.0	169.5
15	DW1	175.0	175.0 (no error)
	DW2	162.5	175.0 (no error)
	PRS31	136.5	150.0
30	DW1	175.0 (no error)	166.0
	DW2	135.5	118.5
	PRS31	85.0	90.5

Table 11 : Maximum bit rate vs. cable length with different patterns

Conclusions

Comparing the results for the various patterns it can be seen, that there is a considerable difference in speed between the values for the short regular patterns (DW1 and DW2) and the long pseudo-random pattern (PRS31). As expected the random pattern yields the worst case results. Therefore only these are considered in the following.
The results in table 11 also show that for cables up to 15 meters long, there is a large speed margin of 35% worst case (15m cable with diode termination) to the target bit rate of 100MBit/s. But for the 30 meter cable the maximum speed is already below 100MBit/s. From the graph in figure 18 we can expect the speed limitation of a 20 meter cable to be about 120 MBit/s for the diode terminated transceiver, and about 130 MBit/s for the resistor terminated transceiver. This still leaves a good speed margin of 20% or 30% respectively.
Apparently, the resistor terminated transceiver can work at higher bit rates, but the difference between the two termination types tends to become smaller for longer cables. It has to be noted though that this is valid under laboratory conditions, and that the diode termination might have some advantages in a more adverse environment (e.g. cable impedance mismatch, strong EMI, common mode injection, etc.).

2.4.2. Measurement with the INMOS Link Test Chip (LTC) TRAM

To confirm the results obtained with the BERT the same measurement was repeated using two INMOS Link Test Chip boards.

Setup

Two LTC-TRAMs were set up for bi-directional link transfer. The high speed clock for the LTC was supplied by a pulse generator. The test pattern consisted of two times 64 random tokens, which were

continuously recirculated by the boards. The test was performed with different length of cable. The measurement procedure used was the same as for the previous test.
The LTC-boards use the 41MGA driver and the 41MF receiver as line buffers. The electrical and timing characteristics are the same as for the 41ML transceiver (used on our test board).

Results

The speed limitation data measured with the LTC is shown in table 12. The graph in figure 18 contains the results obtained with the BERT and with the LTC.

Cable Length [meter]	Pattern	Speed Limitation[MBit/s] D.T.	Speed Limitation[MBit/s] R.T.
1	Random	156.5	160.5
10	Random	144.5	159.5
15	Random	124.0	146.0
30	Random	75.0	81.5

Table 12 : Speed limitation of the INMOS link test chip

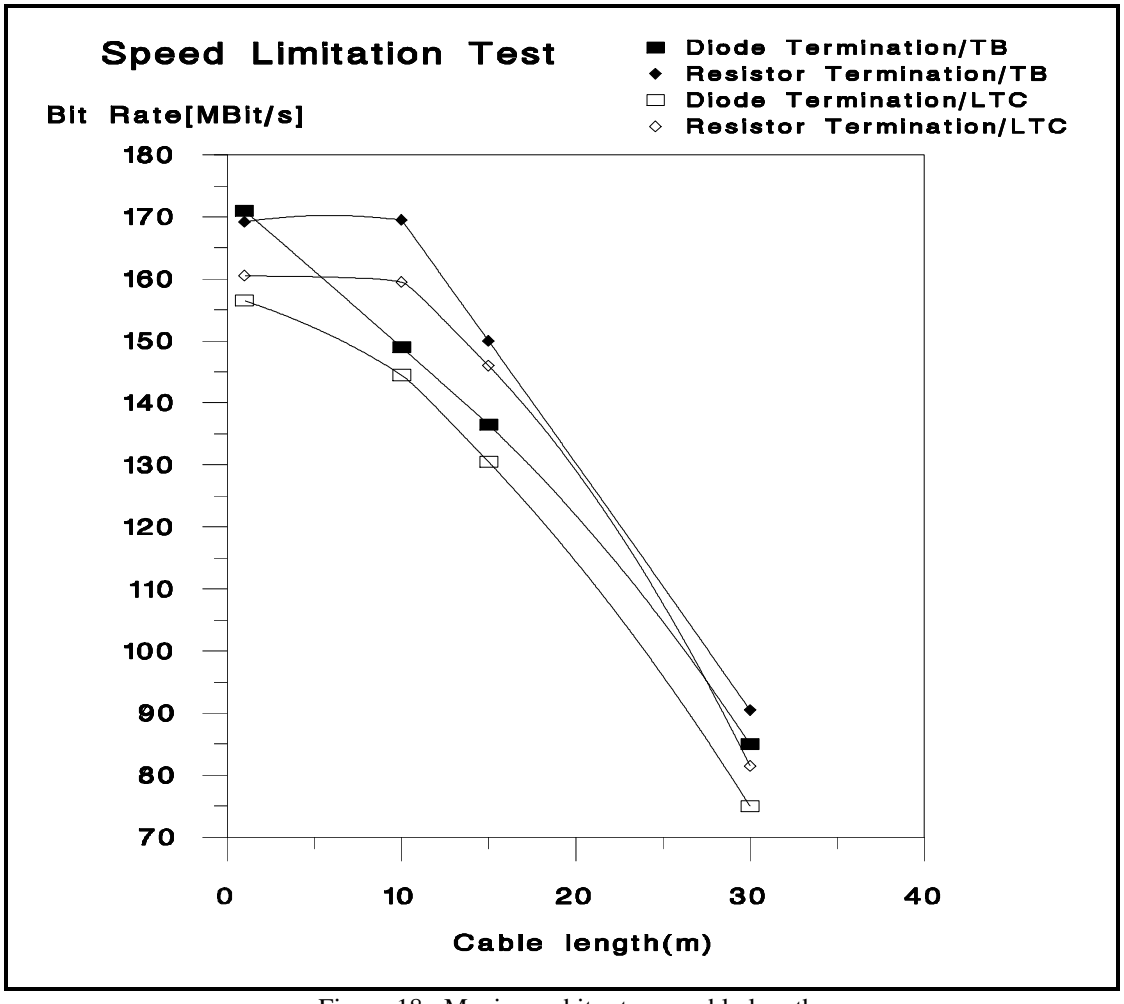

Figure 18 : Maximum bit rate vs. cable length

The graph shows that the results obtained with the BERT and LTC board are very similar, but the actual bit rate values obtained with the LTC are smaller than the ones from the BERT measurement (by about 10%). This is due to the speed limitation of the LTC itself and/or the better input edge resolution of the ECL DS-to-NRZ decoder circuit used on our test boards.

Conclusions

- Transmission at 100MBit/s should be possible with cables of up to 20 meters with a reasonable speed margin of 10% to 25% depending on the termination used.
- The maximum bit rate for a given cable length is about 10% higher for resistor termination.

2.5. Bit Error Rate Test

The previous results were obtained by increasing the bit rate until the transmission failed. This determines an upper limit for the bit rate, but does not give information on long duration error rates in the speed range close to the maximum bit rate. We therefore reduced the speed from the previous measurement by 5% and ran long time error rate tests to demonstrate the reliability of the transmission system.

Setup

The setup is the same as for the speed limitation measurement with the BERT (see figure 17). All the bit rates were reduced by five percent. An error rate test was then run for at least 12 hours at this speed. The test was performed for different length of cable with the pseudo random pattern (PRS31).

Results

cable length [meter]	Pattern	Bit Rate [MBit/s]	Bit Error Rate		Test Time [hr.]	Errors
1	PRS31	166.0	D.T.	1.11E-13	15	0
		165.0	R.T.	7.54E-14	22	0
10	PRS31	145.5	D.T.	1.65E-13	12	0
		165.0	R.T.	1.00E-13	17	0
15	PRS31	130.0	D.T.	1.33E-13	16	0
		145.0	R.T.	2.99E-14	64	0
30	PRS31	81.0	D.T.	2.02E-13	17	0
		86.0	R.T.	1.49E-13	15	0

Table 13 : Bit error rate vs. cable length

Conclusions

All of the above measurement produced no errors, this means that the given bit error rate values have to be regarded as an upper limit for the error rate. It is not possible though, to say how much lower the actual error rate is, this could only be done by prohibitively long test runs (e.g. assuming an error rate of 10^{-15}, at 150Mbit/s it would then take nearly 2000 hours to measure one error). But one can conclude that reducing the bit rate by 20% to 30% (when running at 100MBit/s), instead of by 5%, will result in a very reliable transmission channel.

2.6. Common Mode Measurement

All the previous measurements were carried out with both boards on the same ground voltage level. In practice, when driver and receiver are in different systems, the DC ground levels will be different. Therefore the common-mode range is an important parameter.
The theoretical maximum ground level difference for the case of bi-directional transmission can be calculated as follows : From the data sheet of the AT&T transceiver, the receiver input common mode range is from -1.2V to 7.2V. Using typical values for the high level and low level driver output voltages (Voh = 4.1V, Vol = 3.3V) we can derive the maximum common mode voltage as shown in figure 19. For resistor termination the ground voltage difference can lie between -3.1V and +3.1V.

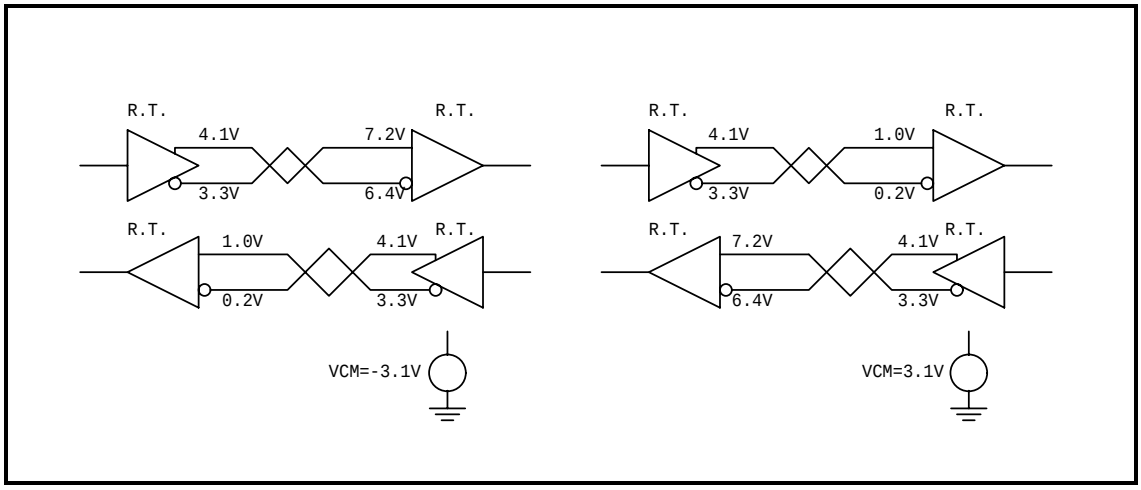

Figure 19 : Maximum common mode voltage for resistor termination

For diode termination, the input voltage of the receiver is limited to the range of -1.2V to 5.6V by the action of protection diodes (see circuit in appendix A1). Therefore the common mode voltage must lie between -1.5V and +1.5V as shown in figure 20.

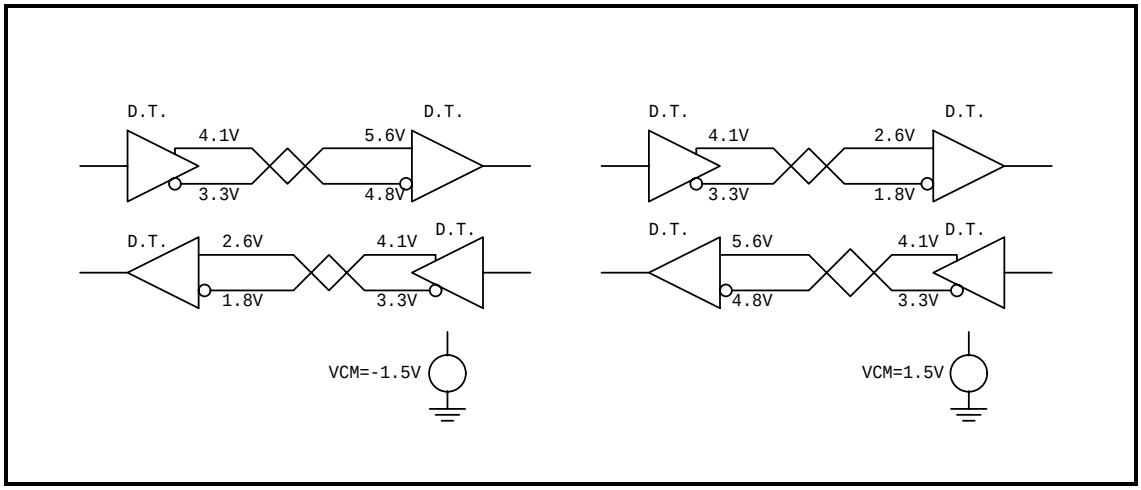

Figure 20 : Maximum common mode voltage for diode termination

It has to be noted that the high and low level output voltages of the driver are not constant as assumed here for the sake of simplicity, but will of course change with the output current and therefore with the common mode voltage.

Setup

The measurement setup is shown below. It allows the two board to work at different DC ground levels (VCM is the ground potential difference). The results were obtained with a bit rate of 100 MBit/s and using a 10 meter cable. The pseudo-random pattern PRS31 was used. The measurement procedure was to increase the common mode voltage until the first bit errors occurred immediately.

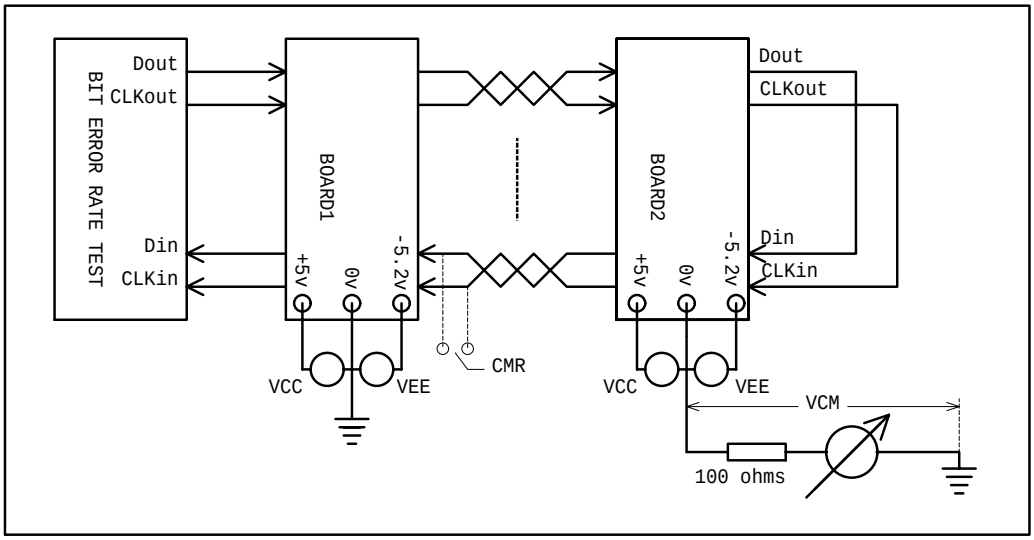

Figure 21 : Common mode measurement

Results

Table 14 shows the measurement results. The difference between the measured common mode voltages and the calculated values can be attributed to the fact that the values used in the calculation are worst case values and that the actual devices perform better.

VCM/D.T.		VCM/R.T.	
Theoretical Data	Measured Data	Theoretical Data	Measured Data
-1.5V	-1.75V	-3.1V	-4.70V
1.5V	1.75V	3.1V	4.75V

Table 14 : Maximum DC ground level difference

Conclusions

It is obvious from the above results, that the range of common mode voltages for the resistor terminated transceiver is more than two times the range for diode termination. The resistor termination does however not contain any protection circuitry. In the measurement setup a resistor was used to limit the maximum current, so that the devices would not be damaged.

3. Conclusion

- DS-link signal transmission using the AT&T differential line drivers/receivers at 100MBit/s works with the chosen cable up to 15m with a very good speed margin. It is expected to run equally well with a 20m cable. Longer length could be reached with a better cable (lower attenuation usually means a thicker cable though).
- The maximum bit rate for a 10 meter cable is 145MBit/s for diode termination and 165MBit/s with resistor termination. Transmission speeds of 200MBit/s could not be reached with our test setup, not even with a short cable length (1 meter). Bit rates up to 200MBit/s might be possible with future implementations of the DS link silicon.
- The performance of the resistor terminated transceiver is better than diode termination in terms of maximum cable length as well as maximum bit rate. This is mainly due to the clamping effect of the schottky-diodes in the termination circuit, which limit the differential input voltage swing.
- There is a significant saving in board space associated with the use of the resistor termination. This also leads to shorter traces on the board for the critical high speed signals.
- As crosstalk does not appear to be a problem, it is not absolutely necessary to use a cable with individually shielded twisted pairs. This is because of the low voltage swing of the PECL signals and the reduced levels of common mode noise or EMI generated by the AT&T devices. Of course differential transmission is also inherently more stable against crosstalk.
- The common mode range of the resistor terminated transceiver is much larger than for the diode terminated one.
- Even though it appears that the performance of the diode termination is inferior to the resistor termination in all aspects, there are some cases where diode termination can be advantageous : If the cable impedance is not well controlled (e.g. using different types of cable), in a very noisy environment, or when protection against large common mode voltages is necessary.
- Mixing the two termination types is possible, the performance would be similar to the performance obtained using diode termination.

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Appendices

A1 Schematics of the Test Board.....I
A2 Data Sheet of 41ML Transceiver II
A3 Waveform Hardcopies III