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HIGH-PERFORMANCE PARALLEL INTERFACE - Serial Specification

(HIPPI-Serial)

working draft proposed
American National Standard

January 19, 1996

Secretariat:

Information Technology Industry Council (ITI)

ABSTRACT: This standard specifies a physical-level interface for transmitting digital data at 800 Mbit/s or 1600 Mbit/s serially over fiber-optic cables across distances of up to 10 km. The signalling sequences and protocol used are compatible with HIPPI-PH, ANSI X3.183-1991, which is limited to 25 m distances. HIPPI-Serial may be integrated as a host's native interface, or used as an external extender for HIPPI-PH ports.

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American National Standard
for Information Systems –

High-Performance Parallel Interface – Serial Specification (HIPPI-Serial)

Secretariat

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Abstract

The described Specification defines a physical-level interface for transmitting digital data at 800 Mbit/s or 1600 Mbit/s serially over fiber-optic cables across distances of up to 10 km. The signalling sequences and protocol used are compatible with HIPPI-PH, ANSI X3.183-1991, which is limited to 25 m distances. HIPPI-Serial may be integrated as a host's native interface, or used as an external extender for HIPPI-PH ports.

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Foreword (This Foreword is not part of American National Standard X3.xxx-199x.)

This High-Performance Parallel Interface, Serial Specification, (HIPPI-Serial) specifies a physical-level interface for transmitting digital data at 800 Mbit/s or 1600 Mbit/s serially over fiber-optic cables across distances of up to 10 km. The signalling sequences and protocol used are compatible with HIPPI-PH, ANSI X3.183-1991, which is limited to 25 m distances. HIPPI-Serial may be integrated as a host's native interface, or used as an external extender for HIPPI-PH ports.

This standard is based on the Serial-HIPPI Specification developed in an ad hoc committee during 1990 through 1993. The ad hoc committee included representatives from computer system manufacturers, peripheral device manufacturers, defense/aerospace equipment manufacturers, communications equipment manufacturers, users of data processing systems, including National Laboratories and Government agencies, as well as others who expressed an interest in developing such a specification. These representatives collectively possessed a considerable knowledge concerning computer interfacing in general, and the HIPPI standards in particular.

Devices conforming to the Serial-HIPPI Specification are now available in the commercial market place, and a desire to more formally document the specification lead to creating this standard. This standard includes enhancements beyond the Serial-HIPPI Specification, e.g., for short-wavelength optics, integrated native host interfaces, and clarifications to some text.

This document includes annexes which are informative and are not considered part of the standard.

Requests for interpretation, suggestions for improvement or addenda, or defect reports are welcome. They should be sent to the X3 Secretariat, Information Technology Industry Council, 1250 Eye Street, NW, Suite 200, Washington, DC 20005.

This standard was processed and approved for submittal to ANSI by Accredited Standards Committee on Information Processing Systems, X3. Committee approval of the standard does not necessarily imply that all committee members voted for approval. At the time it approved this standard, the X3 Committee had the following members:

(List of X3 Committee members to be included in the published standard by the ANSI Editor.)

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Introduction

This High-Performance Parallel Interface, Serial Specification, (HIPPI-Serial) defines a physical-level interface for transmitting digital data at 800 Mbit/s or 1600 Mbit/s serially over fiber-optic cables across distances of up to 10 km. The signalling sequences and protocol used are compatible with HIPPI-PH, ANSI X3.183-1991, which is limited to 25 m distances. HIPPI-Serial may be integrated as a host's native interface, or used as an external extender for HIPPI-PH ports.

Characteristics of a HIPPI Serial interface include:

– Point-to-point connections use one or two pairs of fiber-optic cables for distances of up to 10 km.

– Long wavelength and short wavelength optics options.

– May be used in a simplex or duplex configuration.

– Support for 800 Mbit/s or 1600 Mbit/s data rates.

– Use as an integrated host interface without an intervening HIPPI-PH is supported.

– Use as an external extender for HIPPI-PH ports is supported.

– The coding scheme provides low-latency, automatic link reset, and robust operation.

American National Standard
for Information Technology –

High-Performance Parallel Interface – Serial Specification (HIPPI-Serial)

1 Scope

This American National Standard specifies a physical-level interface for transmitting digital data at 800 Mbit/s or 1600 Mbit/s serially over fiber-optic cables across distances of up to 10 km. The signalling sequences and protocol used are compatible with HIPPI-PH, ANSI X3.183-1991, which is limited to 25 m distances. HIPPI-Serial may be integrated as a host's native interface, or used as an external extender for HIPPI-PH ports.

Specifications are included for:

– the encoding and serialization of the parallel data;

– the sequence of signals required for link reset;

– the timing and optical requirements of the serial signals;

– 32-bit (800 Mbit/s, 100 MByte/s) and 64-bit (1600 Mbit/s, 200 MByte/s) operation;

– simplex and dual simplex operation.

2 Normative references

The following American National Standard contains provisions which, through reference in this text, constitute provisions of this American National Standard. At the time of publication, the edition indicated was valid. All standards are subject to revision, and parties to agreements based on this standard are encouraged to investigate the possibility of applying the most recent edition of the standard listed below.

ANSI X3.183-1991, *High-performance parallel interface, mechanical, electrical, and signalling protocol specification (HIPPI-PH)* .

ANSI X3.230-1994, *Fibre Channel – Physical and Signaling Interface (FC-PH).*

EIA/TIA 492BAAA, *Detail Specification for Class IVa Dispersion Unshifted Single-Mode Optical Waveguide Fibers Used In Communications Systems.*

FOTP-107 (ANSI/EIA/TIA-107-1989), *Return Loss for Fiber Optic Components (February 1989).*

FOTP-127 (ANSI/EIA/TIA-455-127-1991), *Spectral Characteristics of Multimode Laser Diodes Performance, Nov. 1991.*

JIS-C-5973[1], *FO4 Type Connectors for Optical Fiber Cards.*

OFSTP-3 (EIA/TIA-526-3), *Fibre Optic Terminal Equipment Receiver Sensitivity and Maximum Receiver Input, Oct. 1989.*

3 Definitions and conventions

3.1 Definitions

For the purposes of this standard, the following definitions apply.

3.1.1 attenuation: The power loss expressed in units of dB.

[1] JIS documents may be obtained from the Institute of Standardization in Japan.

3.1.2 average power: The optical power measured using an average reading power meter when transmitting continuous valid information.

3.1.3 bit error rate (BER): The statistical probability of a transmitted bit being erroneously received in a communication system. The BER is measured by counting the number of erroneous bits at the output of the receiver and dividing by the total number of bits.

3.1.4 B0-B19: Bits in the 20-bit data field.

3.1.5 center wavelength (laser): The nominal value of the central operating wavelength, defined by a peak mode measurement. (See FOTP-127.)

3.1.6 coding nibble: The 4 bits appended to a 20-bit data field to form a frame. They signal data inversion, indicate fill frames, and supply the Master Transition.

3.1.7 D0-D31, D32-D63: Bits in the 32-bit, and extension for 64-bit, parallel HIPPI word.

3.1.8 data field: The 20-bit data portion of a 24-bit frame.

3.1.9 debounced signal: A signal that has been converted from an intermittent signal to a stable one. (See 7.2.)

3.1.10 Destination: A HIPPI-PH Destination.

3.1.11 extinction ratio: The ratio, expressed in units of dB of the low, or “off” optical power level (PL), to the high, or “on” optical power level (PH), when the station is transmitting valid information.

3.1.12 fiber-optic test procedure (FOTP): Standards developed and published by the Electronic Industries Association (EIA) under the EIA-RS-455 series of standards.

3.1.13 fiber plant: All of the optical elements, for example, fiber, connectors, splices, etc., between an optical transmitter and an optical receiver.

3.1.14 frame: 24 bits consisting of a 20-bit data field and 4-bit coding nibble.

3.1.15 functional unit: A functional partition of the entire system. Partitioning is for the purpose of explanation only. Implementors are free to combine or divide functional units.

3.1.16 HIPPI-PH: High-Performance Parallel Interface - Mechanical, Electrical, and Signalling Protocol Specification (HIPPI-PH), ANSI X3.183-1991. Data is transmitted in parallel over copper twisted-pair cables.

3.1.17 HIPPI port: A HIPPI-PH Source or Destination.

3.1.18 link: One way serial connection between HIPPI-Serial devices.

3.1.19 Master Transition: A bit transition that always appears between the second and third bits of the coding nibble.

3.1.20 mean launch power: The average optical power for a continuous valid information stream coupled into a fiber.

3.1.21 Optical Fiber System Test Practice (OFSTP): Standards developed and published by the Electronics Industries Association (EIA) under the EIA/TIA-526 series of standards.

3.1.22 optical return loss: The ratio (expressed in units of dB) of optical power reflected by a component or an assembly to the optical power incident on a component port when that component or assembly is introduced into a link or system. (See FOTP-107.)

3.1.23 optional: Characteristics that are not required by HIPPI-Serial. However, if any optional characteristic is implemented, it shall be implemented as defined in HIPPI-Serial.

3.1.24 Overhead bit (OH1-OH8): A bit, local to the HIPPI-Serial hardware, which is transmitted along with the HIPPI-PH data over the serial link to provide extra capacity for control and maintenance functions.

3.1.25 Receiver Link Interface (RLI): A functional unit that deserializes and decodes the serial input data into 20-bit data fields.

3.1.26 Source: A HIPPI-PH Source.

3.1.27 spectral width (RMS): The root mean square (RMS) width of the Active Output interface optical spectrum. (See FOTP-127.)

3.1.28 **SUBMUX, SUBDEMUX:** Functional units that combine (extract) the CONNECT, READY, and Overhead bits for transmission across the serial links as bits M0 and M1.

3.1.29 time slot: a contiguous group of 16 frames.

3.1.30 Transmitter Link Interface (TLI): A functional unit that encodes and serializes 20-bit data fields, preparing them for serial transmission.

3.1.31 unit: See functional unit.

3.1.32 XDEMUX: A functional unit that decodes two 20-bit data fields into HIPPI data and control signals.

3.1.33 XMUX: A functional unit that encodes the HIPPI data and control signals into two 20-bit data fields.

3.2 Editorial conventions

In this standard, certain terms that are proper names of signals or similar terms are printed in uppercase to avoid possible confusion with other uses of the same words (e.g., FLAG). Any lowercase uses of these words have the normal technical English meaning.

A number of conditions, sequence parameters, events, states, or similar terms are printed with the first letter of each word in uppercase and the rest lowercase (e.g., State, Source). Any lowercase uses of these words have the normal technical English meaning.

The word *shall* when used in this American National standard, states a mandatory rule or requirement. The word *should* when used in this standard, states a recommendation.

3.3 Acronyms and other abbreviations

BER	bit error rate
dB	decibel
dBm	decibel (relative to 1 mw power)
FOTP	Fiber Optic Test Procedure
HIPPI	High-Performance Parallel Interface
LLRC	Length/Longitudinal Redundancy Checkword
ns	nanoseconds
nm	nanometers
OFSTP	Optical Fiber System Test Practice
PLL	phase locked loop
PRBS	pseudo random bit sequence
RIN	relative intensity noise
RLI	Receiver Link Interface
RMS	root mean square
SUBMUX	Sub Multiplexer
SUBDEMUX	Sub De-Multiplexer
TLI	Transmitter Link Interface
XDEMUX	Receive De-Multiplexer
XMUX	Transmit Multiplexer
µs	microseconds
Ω	ohms

4 System overview

The HIPPI-Serial provides a serial communication facility for HIPPI. The primary purpose of HIPPI-Serial is to extend the physical range of HIPPI beyond 25 meters. A secondary purpose is to replace the parallel HIPPI-PH cable and connectors with a fiber-optic cable.

The primary characteristics of HIPPI-Serial are:

Baud Rate	1.2 GBaud
Maximum station separation:	10 km
Bit-Error Rate	$\leq 10^{-12}$

64-Bit (1600 Mbit/s) HIPPI supported by two HIPPI-Serials in parallel

HIPPI simplex or dual simplex operation

Since error rates are specified to be at or below 10^{-12}, forward error correction, error correcting codes, and CRCs are not addressed in this specification. If additional error detection is deemed necessary, it shall be included as part of the higher level protocols.

4.1 Functional units

Figure 1 is an example showing functional unit building blocks that may be used in a HIPPI-Serial implementation. This specification is written in terms of the functional units shown in figure 1. However, implementors are free to split or combine functions as they choose. This document does not intend to specify any of the interfaces between functional units. The only requirement for compatibility is that the external functionality, at the serial optical interfaces, conform to the overall functionality specified in this document.

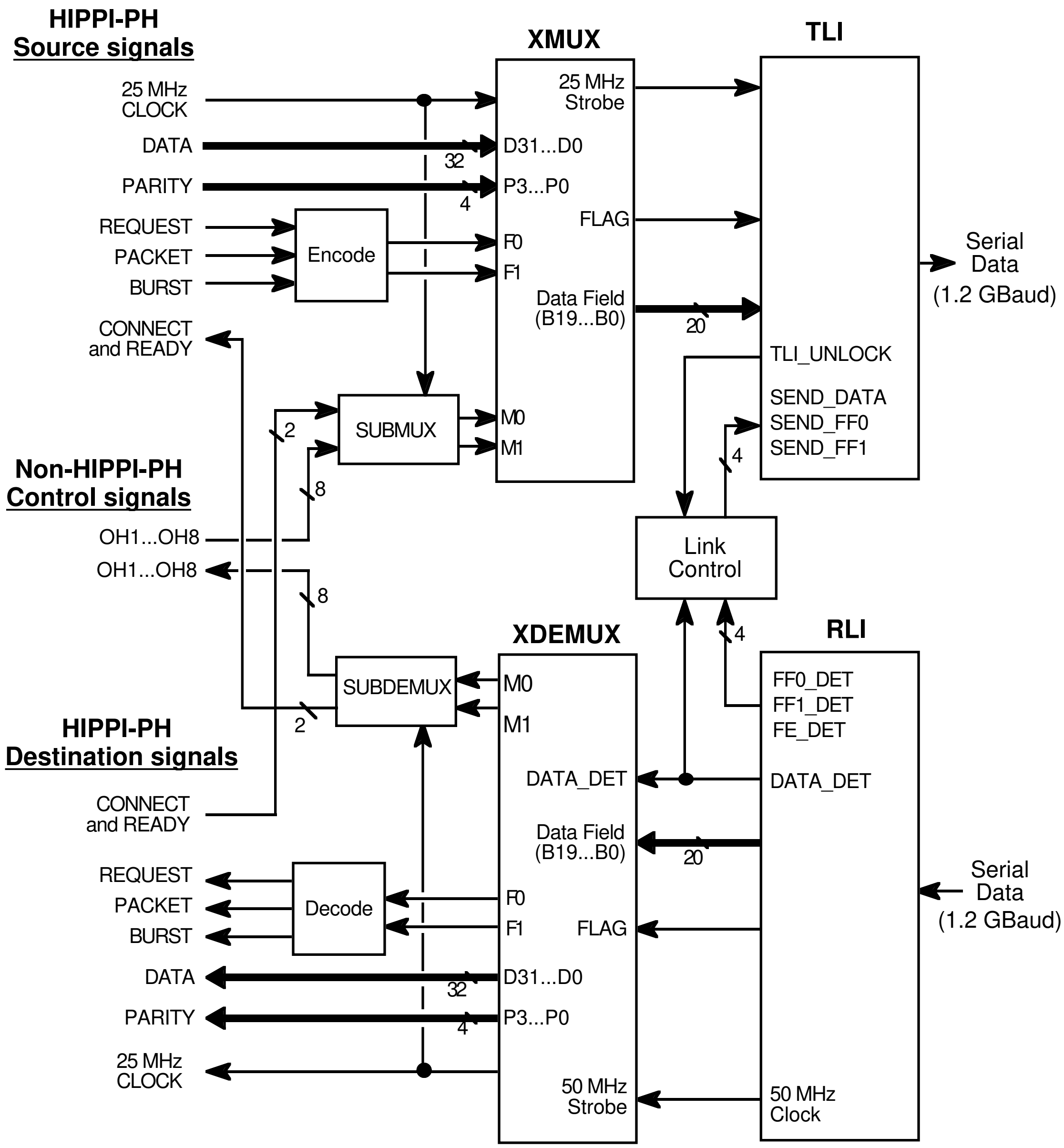

Figure 1 – 32-bit, dual-simplex, HIPPI-Serial functional units example

4.2 HIPPI-PH signals

The HIPPI-PH Source and Destination signals shown in figure 1 shall conform to the signalling protocol specified in ANSI X3.183, HIPPI-PH. These HIPPI-PH signals do not need to conform to the HIPPI-PH mechanical and electrical specifications. The HIPPI-PH INTERCONNECT signals shall not be transported over the serial link to the remote end.

4.3 Non-HIPPI-PH control signals, OH*n* (Overhead bits)

The Overhead bits, OH1 - OH8, provide a framing function and some optional end-to-end status and control capability that is outside the scope of HIPPI-PH. See 5.3.1 for details of the Overhead bits.

4.4 Serial data input and output

The 1.2 GBaud serial data stream defined in this specification is the interoperability point between different implementations.

4.5 Configurations

4.5.1 Dual-simplex and simplex

Figure 1 shows a 32-bit dual-simplex HIPPI-Serial configuration. One fiber cable carries data and control signals from the HIPPI-PH Source, and return direction CONNECT and READY signals to the HIPPI-PH Destination. The other cable carries the reverse direction signals. This uses a pair of links.

Simplex operation may be achieved by ignoring the unused HIPPI-PH signals, or setting them to zeros. The recovered HIPPI-PH CLOCK signal on the active side shall be used to drive the HIPPI-PH Source CLOCK signal on the unused side.

4.5.2 32-bit and 64-bit systems

32-bit (800 Mbit/s) HIPPI-Serial implementations shall use a pair of links and two fibers as shown in figure 1. 64-bit (1600 Mbit/s) HIPPI-Serial implementations shall use two link-pairs shown in figure 1, and four fibers. See 5.1, 6.3, 6.4, and 6.5 for details of the information on the separate links of a 64-bit implementation. See 7.3 for details of the 64-bit dual-link reset operations.

4.5.3 HIPPI-Serial extenders

An external extender for copper-cable-based HIPPI-PH ports is described in annex D.

5 Transmit section

The transmit section consists of the Encode, SUBMUX, XMUX, and Transmitter Link Interface (TLI) functional units shown in the top portion of figure 1. The transmit section encodes parallel signals into a DC balanced serial stream.

5.1 Encoding the 20-bit data fields

40-bit words consisting of 32 bits of HIPPI-PH data, 4 bits of HIPPI-PH parity, F0, F1, M0, and M1, shall be split into two 20-bit data fields. In figure 1 this function is called the XMUX. A FLAG signal shall be used to identify the first 20-bit data field from the second 20-bit data field. Table 1 specifies the bit assignments in the 20-bit data fields, and the associated FLAG values. The 20-bit data field with FLAG = 0 shall be transmitted before the related 20-bit data field with FLAG = 1.

NOTE – The bit arrangement in table 1 reduces the possibility of corrupted data being identified as good data. The HIPPI-PH parity bits cover a byte of adjacent data bits, e.g., P0 covers D0 - D7. By scattering the HIPPI-PH data and parity bits in the 20-bit words, a noise hit corrupting up to seven adjacent data field bits in the serial stream will be detected as a HIPPI-PH parity error. Corrupted bits in the coding nibble, will also be detected as errors.

32-bit (800 Mbit/s) HIPPI-Serial variants shall use one link as shown in figure 1, and shown as link "a" in table 1.

64-bit (1600 Mbit/s) HIPPI-Serial variants shall use two separate physical links in parallel; called links "a" and "b" in table 1. The serial data streams on links "a" and "b" shall be time aligned within 2 ns at the transmitter.

Table 1 – 20-bit data field structure

Link - FLAG	Data field bit B*n*																			
	0	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**
a - 0	D00	D08	D16	D24	D01	D09	D17	D25	D02	D10	D18	D26	D03	D11	F0	D19	D27	P0	P1	F1
a - 1	P2	P3	D04	D12	D20	D28	D05	D13	D21	D29	D06	D14	D22	D30	M0	D07	D15	D23	D31	M1
b - 0	D32	D40	D48	D56	D33	D41	D49	D57	D34	D42	D50	D58	D35	D43	F0	D51	D59	P4	P5	F1
b - 1	P6	P7	D36	D44	D52	D60	D37	D45	D53	D61	D38	D46	D54	D62	'0'	D39	D47	D55	D63	'0'

Link: *a/b* denotes separate physical links. *a* is used individually for 800 Mbit/s operation, *a* and *b* are used together for 1600 Mbit/s operation.
FLAG: *0/1* is derived from the coding nibble and is used to differentiate the first and second 20-bit data fields of a 40-bit word.
D*nn* = HIPPI data bit
P*n* = HIPPI parity bit
F0, F1 = REQUEST, BURST, and PACKET encoding (See 5.4 and table 2.)
M0, M1 = Submultiplexed CONNECT, READY, and Overhead signals (See 5.5.)

5.2 Encoding F0, F1 with REQUEST, PACKET, and BURST

The HIPPI-PH REQUEST, PACKET, and BURST control signals shall be encoded into the F0 and F1 bits as shown in table 2. (See annex C.1 for descriptions of these HIPPI-PH signals.)

Table 2 – REQUEST, PACKET and BURST coding in F0 and F1

HIPPI-PH signals			Code		
REQUEST	**PACKET**	**BURST**	**F1**	**F0**	**State**
0	0	0	0	0	Idle
1	0	0	0	1	Request
1	1	0	1	0	Packet
1	1	1	1	1	Burst
0	0	1	0	0	Idle
0	1	0	0	0	Idle
0	1	1	0	0	Idle
1	0	1	0	0	Idle

5.3 Encoding M0, M1 with CONNECT, READY, and OH*n*

The M0 and M1 bits carry several lower-bandwidth signals multiplexed together. Table 3 shows the signals, and their relative frames. An example circuit to generate the M0 and M1 signals is described in annex A.1 and shown in figure A.1. This function is called the SUBMUX in figure 1.

NOTE 1 – A pair of 20-bit data fields are transferred over a link every 40 ns, corresponding to the 25 MHz HIPPI-PH CLOCK signal. For example, D0-D31, P0-P3, REQUEST, PACKET, BURST, M0 and M1, are transmitted every 40 ns. At relative frame 0, M0 would have the first sample of "READY a", 40 ns later (relative frame 1) M0 would have the second "READY a", at 80 ns (relative frame 2) M0 would have the third "READY a", at 120 ns (relative frame 3) M0 would have the OH5 signal, etc. Relative frame 0 is not synchronized with any specific HIPPI-PH signal combination or transition, i.e., its location is arbitrary.

Table 3 – M0, M1 contents

Relative Frame	M0 contents	M1 contents
0	READY a	CONNECT a
1	READY a	CONNECT a
2	READY a	CONNECT a
3	OH5	OH1
4	READY b	CONNECT b
5	READY b	CONNECT b
6	READY b	CONNECT b
7	OH6	OH2
8	READY c	CONNECT c
9	READY c	CONNECT c
10	READY c	CONNECT c
11	OH7	OH3
12	READY d	CONNECT d
13	READY d	CONNECT d
14	READY d	CONNECT d
15	OH8 (Alt 0/1)	OH4

Each of the three adjacent CONNECT or READY bits, e.g., READY a, READY a, and READY a, shall be transmitted with the same value.

NOTE 2 – The HIPPI-PH CONNECT and READY signals travel in the reverse direction from the data and other HIPPI-PH signals, without a reference clock or checksum. To improve the reliability of the CONNECT and READY signals in HIPPI-Serial, they are sent three times, e.g., the three READY a's, and spaced 40 bits apart in the serial stream. Majority voting logic at the receiver will correct most of the serial steam M0 and M1 errors associated with the CONNECT and READY signals.

5.3.1 OH*n* (Overhead bits)

Table 4 lists the Overhead bits. If optional Overhead bits are used, their functions shall be as specified in table 4. If an optional function is not used, then its bit shall be transmitted as the default value shown in table 4. The OH8 bit shall be an alternating 1/0 pattern to provide framing for the Overhead bit stream.

Table 4 – Overhead bit (OH*n*) functions

OH Bit	Default Value	Opt/ Man	Function
OH1	0	Opt	Link Status and Control
OH2	0	Opt	Asynchronous channel
OH3	0	Opt	Asynchronous channel
OH4	0	Opt	Reserved
OH5	0	Opt	Reserved
OH6	0	Opt	Vendor unique
OH7	1	Opt	Vendor unique
OH8	1/0	Man	Framing (alternate 1/0)

OH = Overhead
Opt = Optional
Man = Mandatory

NOTE – The optional functions assigned seem appropriate for HIPPI-Serial Extenders as described in annex D, but may not be appropriate for HIPPI-Serial integrated in a workstation.

5.3.2 Overhead bit OH1 encoding

Table 5 defines the functions carried in optional Overhead bit 1 (OH1). Like M0 and M1, OH1 carries lower bandwidth signals multiplexed in time slots. If an optional function of OH1 is not used, then the default value shown in table 5 shall be transmitted in that OH1 time slot.

Table 5 – Overhead bit 1 (OH1) coding

Time Slot	Default Value	Opt/ Man	Function
0	1	Man	Framing
1	1	Man	Framing
2	1	Man	Framing
3	1	Man	Framing
4	0	Man	Framing
5	0	Opt	RL: Remote loopback
6	0	Opt	PP: Parallel Parity Error
7	0	Opt	SP: Serial Parity Error

Opt = Optional
Man = Mandatory when OH1 is used

RL: Remote Loopback - (Optional) If one end of a link desires the other end to go into remote loopback, it shall transmit bit RL as a 1. When RL is received as a 1, the receiving node should go into remote loopback. When in remote loopback, all data received shall be echoed back to the other end of the link, including the RL signal itself. (This will acknowledge that the link is in remote loopback, and will allow the echoed data to be checked for errors.) RL is a level sensitive, static signal. As long as it is 0, the link operates normally. As long as it is received as a 1, the node should echo all received data. However, RL should be filtered to prevent infrequent bit errors from falsely enabling loopback. When an end initiates remote loopback, it shall not go into remote loopback upon receiving RL = 1. For recommended implementations of loopback, refer to annex D.2.

PP: Parallel Parity Error - (Optional) Any parity errors detected on the Source HIPPI-PH data should be flagged by transmitting PP as a 1. PP shall be stretched to between 6 µs and 9 µs to guarantee transmission over the link. The status of PP should be made available at both the local and remote ends of the link. Persistent parallel parity errors indicate a problem with the HIPPI-PH Source port.

SP: Serial Parity Error - (Optional) The parity of the HIPPI-PH data should be checked once again as it is delivered from the XDEMUX in figure 1 to the HIPPI-PH Destination. An error at this point should be flagged by setting SP of the transmit link to a 1. The status of SP should be made available at the local end of the link, and it should be transmitted back to the remote node if a duplex system is in use. SP shall be stretched to between 6 µs and 9 µs to guarantee transmission over the link. Assuming the transmitted Parallel Parity Error signal (PP) is 0, persistent received Serial Parity Errors (SP = 1) indicate a problem with the serial transmit portion of the link.

5.3.3 Overhead bits OH2, OH3 encoding

When implemented, OH2 and OH3 provide 195 KBaud bit streams that may be used for end-to-end voice or data signalling separate from HIPPI-PH traffic. Each OH2 and OH3 value transmitted shall cover at least eight time slots, i.e., at least 5.12 µs. When implemented, OH2 and OH3 shall be transmitted as a 1 when there is no other data to be transmitted.

5.4 Converting parallel data to serial

Converting from parallel to serial occurs in the Transmitter Link Interface (TLI) functional unit shown in figure 1. Table 6 defines the 24-bit frames that will be serialized by the TLI.

The bits in table 6 shall be transmitted in a left to right sequence, i.e., B0 shall be transmitted first; C3 transmitted last. The data shall be transmitted in a non-return to zero fashion, i.e., 1 = light on, 0 = light off.

The Link Control functional unit controls the types of frames transmitted with the signals:

SEND_DATA: Transmit Data Frame

SEND_FF0: Transmit Fill Frame 0s

SEND_FF1: Transmit Fill Frame 1s

DC balance shall be achieved by keeping the number of 1s transmitted as close as possible to the number of 0s transmitted. A running count shall be kept of the number of 1s and 0s transmitted in the serial stream, counting the DISPARITY counter up for each 1 transmitted, and counting down for each 0 transmitted. The initialization point for the DISPARITY counter shall be when SEND_FF0 transitions from true to false.

NOTE – The DISPARITY counter can be implemented with an up/down counter with a range of plus or minus 31.

5.4.1 Transmit Data Frame

When SEND_DATA = true, and there is a 20-bit data field to transmit, then the TLI shall append a 4-bit coding nibble to the 20-bit data field; if FLAG = 0 then coding nibble = 1101, if FLAG = 1 then coding nibble = 1011.

DC balance shall be achieved by keeping the number of 1s transmitted as close as possible to the number of 0s transmitted. As with the DISPARITY counter, the number of 1s and 0s in each 24-bit Data Frame to be sent shall be counted in the NEW counter. The NEW counter shall be initialized for each new 24-bit Data Frame; it is not a running count of all 24-bit Data Frames transmitted. If the sign of the NEW counter is the same as the sign of the DISPARITY counter, then the bits in the 24-bit Data Frame shall be inverted before being transmitted serially. For example, compare the first two rows in table 6.

5.4.2 Transmit Fill Frame 0

When SEND_FF0 = true, the TLI shall transmit 24-bit Fill Frame 0s (FF0) as defined in table 6. Since FF0 has an equal number of 1s and 0s, it is already DC balanced. FF0s are used during a link reset operation. (See 7.3.1.)

5.4.3 Transmit Fill Frame 1

When SEND_FF1 = true, the TLI shall transmit 24-bit Fill Frame 1s (FF1) as defined in table 6. SEND_FF1 = true occurs during a link reset operation. (See 7.3.2.)

Note that in table 6 there are two Fill Frame 1s, FF1H and FF1L. FF1H contains more 1s than 0s, and FF1L contains more 0s than 1s. To achieve DC balance FF1Ls shall be transmitted when the sign of the DISPARITY counter is positive, and FF1Hs shall be transmitted when the sign of the DISPARITY counter is negative.

5.5 Transmit section clock signals

The serial data stream shall be transmitted at a rate of 48 times the HIPPI-PH CLOCK rate, i.e., 48 x 25 MBaud = 1.2 GBaud. The TLI shall set TLI_UNLOCK = 0 when the TLI clock multiplier is stable and locked.

Table 6 – 24-bit frame structure

24-bit frame: Data field (B0 … B19)	Coding nibble C0	C1	C2	C3	Interpretation
XXXXXXXXXXXXXXXXXXXX	1	1	0	1	Data Frame, FLAG = 0, Data True
$\overline{\text{XXXXXXXXXXXXXXXXXXXX}}$	0	0	1	0	Data Frame, FLAG = 0, Data Inverted
XXXXXXXXXXXXXXXXXXXX	1	0	1	1	Data Frame, FLAG = 1, Data True
$\overline{\text{XXXXXXXXXXXXXXXXXXXX}}$	0	1	0	0	Data Frame, FLAG = 1, Data Inverted
11111111110000000000	0	0	1	1	Fill Frame 0 (FF0)
11111111111000000000	0	0	1	1	Fill Frame 1, Heavy (FF1H)
11111111100000000000	0	0	1	1	Fill Frame 1, Light (FF1L)
XXXXXXXXX10XXXXXXXXX	1	1	0	0	Reserved Frame
XXXXXXXXX01XXXXXXXXX	0	0	1	1	Reserved Frame
XXXXXXXXX0XXXXXXXXXX	1	1	0	0	Frame Error
XXXXXXXXX11XXXXXXXXX	1	1	0	0	Frame Error
XXXXXXXXXXXXXXXXXXXX	1	0	1	0	Frame Error
XXXXXXXXXXXXXXXXXXXX	0	1	0	1	Frame Error
XXXXXXXXXXXXXXXXXXXX	X	0	0	X	Frame Error (no Master Transition)
XXXXXXXXXXXXXXXXXXXX	X	1	1	X	Frame Error (no Master Transition)

6 Receive section

The receive section consists of the Receiver Link Interface (RLI), XDEMUX, SUBDEMUX, and Decode functional units shown in the lower portion of figure 1. The receive section decodes the serial stream, frames the signals, checks for errors, and outputs parallel signals.

6.1 Receive section clock signals

Note that the FF0 pattern in table 6 results in a square wave with 12 consecutive 1s followed by 12 consecutive 0s. Also notice that a 1 to 0, or 0 to 1, transition, called the Master Transition, occurs at the coding nibble bits C1 to C2. The Master Transition shall be used for synchronizing the Master Transition Clock, and shall be used to frame groups of 24 bits into the 24-bit words shown in table 6. The Master Transition Clock shall be locked to the Master Transitions in the received serial data stream, e.g., with a phase locked loop. The received serial data stream shall be strobed at a rate of 24 times the Master Transition Clock rate to recover the bits.

NOTES
1 The Master Transition Clock rate is initially derived from the FF0 square wave during the reset operation. (See 7.3.1.) When passing data, the Master Transition Clock rate is maintained by synchronizing to the Master Transition occurring every 24 bits.

2 The Master Transition Clock should have the same long-term tolerance as the HIPPI-PH CLOCK signal since it is directly derived from it. HIPPI-PH specifies a ± 0.01% tolerance for the transmitted CLOCK signal.

3 The Master Transition Clock rate is twice the HIPPI-PH CLOCK rate, i.e., 50 MHz. The bit clock rate for strobing the received serial data stream operates at 24 times that rate, i.e., 1.2 GHz.

4 A clock recovery circuit for 50 MHz should be simpler than for a 1.2 GHz. A simple, easily integrated, Phase Locked Loop (PLL) clock recovery mechanism utilizing this Master Transition is described in references [1-5] in annex E.

6.2 Operating on the 24-bit frames

The RLI shall signal the type of 24-bit frame received based on the values in table 6. Only one of the following signals shall be true for each 24-bit frame received.

DATA_DET: a Data Frame was detected

FF0_DET: an FF0 was detected

FF1_DET: an FF1H or FF1L was detected

FE_DET: a Frame Error was detected

Reserved Frames should never be sent or received, but future enhancements to HIPPI-Serial may define uses for the reserved frames. Any reserved frames received shall be discarded without interpretation. Violations of this guideline may result in loss of upward compatibility.

6.2.1 Receiving Data Frames

A 24-bit frame with a binary coding nibble value of 1101, 0010, 1011, or 0100, i.e., the first four rows of table 6, is called a Data Frame. If the coding nibble of a Data Frame indicates that the data is inverted, then the 20-bit data field shall be inverted before being passed to the XDEMUX. The FLAG signal shall also be derived from the coding nibble as defined in table 6.

6.2.2 Receiving Fill Frame 0 (FF0)

Receiving an FF0 indicates that a reset operation is underway. (See 7.3.1.) The REQUEST, PACKET, BURST, signals to the HIPPI-PH Destination, and the READY and CONNECT signals to the HIPPI-PH Source, shall be set to zeros. A parity error shall be forced in the data sent to the HIPPI-PH Destination.

NOTE – A simple way to force parity errors in a given HIPPI word is to set all of the data and parity bits to the HIPPI-PH Destination to 0. Because HIPPI-PH uses odd parity, all four parity bits will appear to have parity errors.

6.2.3 Receiving Fill Frame 1 (FF1)

Receiving a FF1 indicates that a reset operation is underway. (See 7.3.2.) The REQUEST, PACKET, BURST, signals to the HIPPI-PH

Destination, and the READY and CONNECT signals to the HIPPI-PH Source, shall be set to zeros. A parity error shall be forced in the data sent to the HIPPI-PH Destination.

6.2.4 Receiving Frame Errors

A Frame Error, FE_DET, as defined in table 6, shall cause the following:

– A parity error shall be forced in the data sent to the HIPPI-PH Destination.

– The HIPPI-PH REQUEST, PACKET, and BURST signals to the HIPPI-PH Destination shall be maintained at their previous values. See annex C.2 for a discussion of ramifications of maintaining these signals at the previous value.

– The M0/M1 time slot shall be advanced, and the functions encoded in M0 and M1 shall be maintained at their last value.

– Two consecutive Frame Errors shall cause the link to be reset. (See 7.3.1 for reset details.)

6.3 Decoding 20-bit data fields

The 20-bit data fields signalled by DATA_DET = 1 are processed by the XDEMUX functional unit shown in figure 1. The 20-bit data field with FLAG =0, and the following 20-bit data field with FLAG = 1 shall be combined to form a 40-bit words. The 40-bit words shall be decoded as defined in table 1.

As specified in 4.5.2, 32-bit (800 Mbit/s) HIPPI-Serial variants use only one link as shown in figure 1, and shown as link "a" in table 1, i.e., the 40-bit words correspond to HIPPI data bits D00 - D31.

As specified in 4.5.2, 64-bit (1600 Mbit/s) HIPPI-Serial variants use two separate physical links in parallel; called links "a" and "b" in table 1. The serial data stream on fiber "a" carries HIPPI data bits D00 - D31. The separate serial data stream on fiber "b" carries HIPPI data bits D32 - D63. The F0 and F1 signals present in both the "a" and "b" links shall be used to time synchronize the two links, i.e., get the right D00 - D31 and D32 - D63 together. The serial data streams on links "a" and "b" shall be time aligned, by matching or trimming the cable lengths, so that there is ≤ 22 ns between F0 on cable "a" and F0 on cable "b".

6.4 Decoding F0, F1 into REQUEST, PACKET, and BURST

The F0 and F1 bits of the 40-bit word shall be decoded into the REQUEST, PACKET, and BURST signals as defined in table 2. The REQUEST, PACKET and BURST signals shall be transmitted to the HIPPI Destination on the same CLOCK used to transmit the HIPPI data signals of that 40-bit word. This function is done in the Decode functional unit of figure 1.

64-bit (1600 Mbit/s) HIPPI-Serial variants shall use only the F0 and F1 signals from the "a" link to decode the HIPPI-PH REQUEST, PACKET, and BURST signals.

6.5 Decoding M0, M1 into CONNECT, READY, and OH*n*

The M0 and M1 bits of the 40-bit word shall be used to decode the CONNECT, READY, and Overhead bits as defined in table 3. Note that multiple occurrences of the M0 and M1 bits are required to construct the CONNECT and READY signals. A four-HIPPI-PH-CLOCK-cycle wide READY indication shall be transmitted to the HIPPI Source if two out of three READY "n" signals = 1, where n = a, b, or c. CONNECT signals shall be processed in the same manner. The CONNECT and READY signals, without further processing, shall meet the requirements of X3.183, HIPPI-PH, i.e., be careful of their relative timing on the transmit side. There is no requirement that CONNECT or READY be passed to the HIPPI Source with the same CLOCK used to transfer the HIPPI data signals of that 40-bit word. An example circuit to decode the M0 and M1 signals is described in annex A.2 and shown in figure A.2. This function is called the SUBDEMUX in figure 1.

NOTE – The bits corresponding to M0 and M1 on link "a" are held to zero on link "b". This ensures that a 64-bit (1600 Mbit/s) HIPPI-Serial variant will not operate if the cables are reversed, i.e., CONNECT and READY will never be true.

7 Link Control

7.1 Link Control output signals

The Link Control functional unit is shown in figure 1. There are identical Link Control functional units at the local and remote ends of a link. For the purposes of describing some of the HIPPI-Serial operations, the following logical output signals from the Link Control functional unit are assumed:

SEND_DATA - Signals the TLI to transmit Data Frames. (See 5.4.1.)

SEND_FF0 - Signals the TLI to transmit FF0. (See 5.4.2.)

SEND_FF1 - Signals the TLI to transmit FF1H or FF1L. (See 5.4.3.)

7.2 Link Control input signals

Likewise, the following logical input signals to the Link Control functional unit are assumed:

DATA_DET - Indicates that the RLI has detected a Data Frame. (See 6.2.1.)

FF0_DET - Indicates that the RLI has detected a Fill Frame 0 (FF0). (See 6.2.2.)

FF1_DET - Indicates that the RLI has detected a Fill Frame 1 (FF1H or FF1L). (See 6.2.3.)

FE_DET - Indicates that the RLI has detected a Frame Error. (See 6.2.4.)

TLI_UNLOCK – Indicates that the clock multiplier in the TLI is not locked. (See 5.5.)

Single bit errors in the received serial stream can cause FF0s, FF1s, and Data Frames to be confused. Therefore, FF0, FF1, and FE_DET shall only be considered true when two consecutive frames give the same indication. In this specification, this two consecutive indications is called a debounced signal.

7.3 Link reset

The links shall be reset at power-on, and when two consecutive Frame Errors are detected as specified in 6.2.4. The Link reset state diagram, as shown in figure 2, consists of three states. The states are uniquely defined by the serial data stream contents transmitted by the TLI when the Link Control functional unit is in that state.

The conditions to leave each state are shown next to the arrows between states. For clarity, the conditions that cause the Link Control functional unit to remain in a given state are shown on an arrow that loops back to the same state.

32-bit, (800 Mbit/s) simplex, and dual-simplex, configurations use a pair of links, and 64-bit (1600 Mbit/s) HIPPI-Serial variants use two link-pairs. Each pair of links independently executes this same reset procedure.

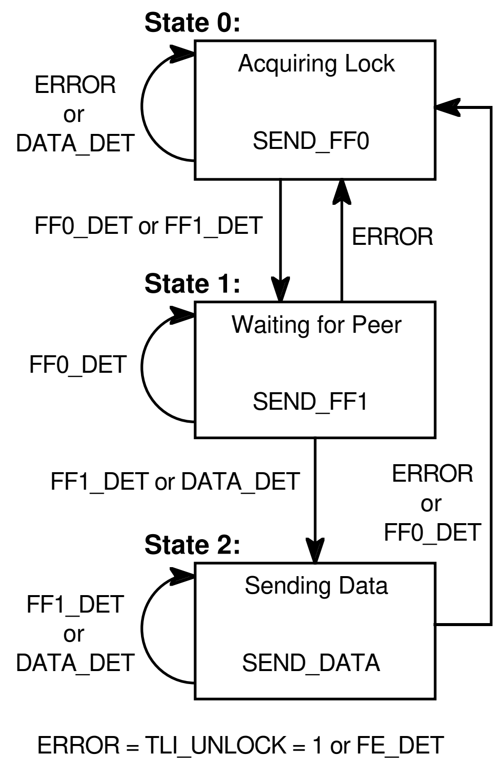

Figure 2 – Link reset state diagram

7.3.1 State 0: Acquiring Lock

In this State the TLI is transmitting a 50 MHz square wave, i.e., FF0, to initialize the clock recovery circuitry at the remote end RLI, and the local RLI is locking onto a similar incoming signal. All of the control signals to the HIPPI ports shall be held deasserted, and the control signals from the HIPPI ports shall be ignored. After the transmit clock is stable and locked, i.e., TLI_UNLOCK = 0, the TLI shall transmit FF0 across the link for at least 128 frame times (2.56 µs) . The Link Control functional unit shall go to State 1 when its local RLI has achieved lock and framing, i.e., it detects debounced FF0s or FF1s, and no FE_DETs, for at least 128 frame times (2.56 µs).

7.3.2 State 1: Waiting for Peer

In this state the node is ready to go, but is waiting for the other end of the link. All of the control signals to the HIPPI ports shall be held deasserted, and the control signals from the HIPPI ports shall be ignored. The local TLI shall transmit FF1 to the other end of the link to signal that it is ready. The local node knows the other end of the link is not ready, because it is still receiving FF0. Upon receipt of debounced FF1s or Data Frames, it will know that the other end of the link is locked and ready to go. In that case the local node shall go to State 2.

7.3.3 State 2: Sending Data

In this state the TLI sends continuous Data Frames. The Link Control functional unit shall remain in this state indefinitely, until a debounced ERROR or FF0 is detected. In that case, the link shall return to State 0, and the reset procedure begins again.

Until at least 20 µs after State 2 is reached, the CONNECT and READY signals shall be held to zeroes. Holding the control signals to defined values avoids confusing signals to the HIPPI ports, and the 20 µs delay allows enough time to frame the M0 and M1 signals.

8 Serial optical interface

8.1 General specifications

Tables 7 to 9 include the relevant specifications for the optical interfaces and components for compatibility with HIPPI-Serial at both the long and short wavelengths. Optical 10% and 90% transition times shall be measured using a Fill Frame 0 (FF0) pattern.

8.1.1 Optical output interface

The general laser transmitter pulse shape characteristics are specified in the form of a mask of the transmitter eye diagram. These characteristics include rise time, fall time, pulse overshoot, pulse undershoot, and ringing, all of which should be controlled to prevent excessive degradation of the receiver sensitivity. The parameters specifying the mask of the transmitter eye diagram are shown in figure 3.

The mask of the eye diagram for the laser transmitters shall be measured using a receiver with a fourth-order Bessel-Thompson transfer function that has a 3 dB of attenuation at the reference frequency (f_r) of:

$$f_r = 0.75 \text{ x Bit Rate}$$

NOTE – This filter is not intended to represent the noise filter used within an optical receiver but it is intended to provide a uniform measurement condition. A SONET OC-24, or a Fibre Channel 1062.5 MBaud, reference filter meets the necessary requirements when coupled to a wide band optical receiver.

8.1.2 Optical input interface

The receiver shall operate at a BER $\leq 10^{-12}$ over the link's lifetime and temperature range when the input power falls in the range given in tables 7 to 9 and when driven by a data stream output that fits the specified eye diagram mask through a cable plant as specified in tables 7 to 9. The measurement shall be made by the methods of OFSTP-3 (EIA/TIA-526-3).

The minimum and maximum values of the average received power in dB give the input power range to maintain a BER $\leq 10^{-12}$. These values take into account power penalties caused by the use of a transmitter with worst-case combination of transmitter spectral, extinction ratio, and pulse shape characteristics. The receiver sensitivity does not include power penalties associated with dispersion, jitter, or reflections from the optical path; these effects are specified separately in the allocation of maximum optical path penalty. (See annex B.5 for loss budget examples.)

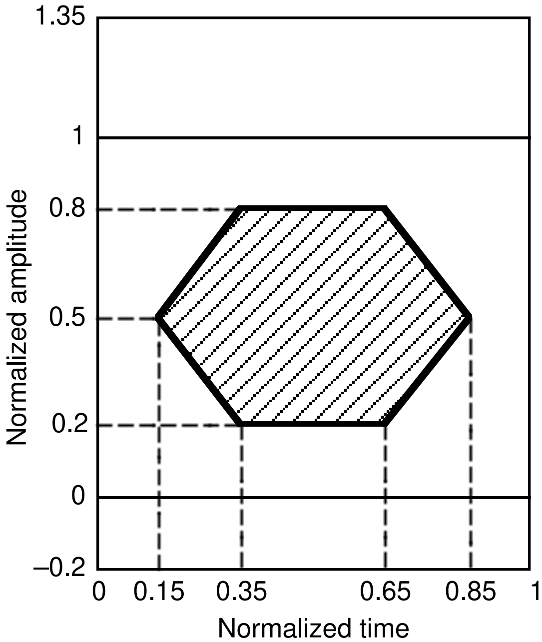

Figure 3 – Transmitter eye diagram mask

8.2 Fiber type

The single-mode optical fiber shall conform to EIA/TIA 492BAAA. The multimode optical fiber may be either 50 or 62.5 µm. Mixing 50 and 62.5 µm optical fiber in a single link is not allowed.

8.3 Optical connectors

Duplex SC connectors, as defined in ANSI X3.230 and JIS-C-5973, are recommended. FC/PC and ST connectors are optional.

Table 7 – General long wavelength optical specifications over single-mode fiber

System rate, length, and BER	
Baud rate	1.2 GBaud
Distance	≤ 10 km
Optical fiber	Single mode
BER (max)	1 x 10^{-12}
Optical transmitter (at output connector)	
Transmitter type	Pigtailed laser
Center wavelength	1285 to 1330 nm
Maximum spectral width (RMS)	3 nm
Mean launch power	–9 to –6 dBm
Allowable extinction ratio	8 to 20 dB
Optical 10 to 90% transition times	≤ 300 ps
RIN (max)	–116 dB/Hz
Optical input to optical receiver	
Received optical power	–22 to –6 dBm
Allowable extinction ratio	8 to 20 dB
Receiver return loss	≥ 40 dB
Discrete connector return loss	≥ 30 dB
Optical 10 to 90% transition time	≤ 360 ps
Optical path	
Optical fiber core diameter	8 to 10 µm
Zero dispersion wavelength	1310 ± 10 nm
Maximum dispersion	3.5 ps/(nm x km)
Slope at zero dispersion	0.095 ps/(km x nm^2)
Maximum cable loss	0.5 dB/km
Mean fiber plant attenuation (DC)	0 to 9 dB
Discrete connector return loss	≥ 30 dB
Recommended connector	Duplex SC
Optional connectors	FC/PC or ST

Table 8 – General long wavelength optical specifications over multimode fiber

System rate, length, and BER	
Baud rate	1.2 GBaud
Distance	≤ 1 km
Optical fiber	50 and 62.5 µm multimode
BER (max)	1 x 10^{-12}
Optical transmitter (at output connector)	
Transmitter type	Pigtailed laser
Center wavelength	1285 to 1330 nm
Maximum spectral width (RMS)	3 nm
Mean launch power	–9 to –6 dBm
Allowable extinction ratio	8 to 20 dB
Optical 10 to 90% transition times	≤ 300 ps
RIN (max)	–116 dB/Hz
Optical input to optical receiver	
Received optical power	–22 to –6 dBm
Allowable extinction ratio	8 to 20 dB
Receiver return loss	≥ 40 dB
Discrete connector return loss	≥ 30 dB
Optical 10 to 90% transition time	≤ 360 ps
Optical path	
Optical fiber core diameter	50 or 62.5 µm
Minimum bandwidth	450 MHz · km
Mean fiber plant attenuation (DC)	0 to 9 dB
Discrete connector return loss	≥ 30 dB
Recommended connector	Duplex SC
Optional connectors	FC/PC or ST

Table 9 – General short wavelength optical specifications

System rate, length, and BER	
Baud rate	1.2 GBaud
Distance:	
62.5 µm optical fiber	≤ 300 m
50 µm optical fiber	≤500 m
BER (max)	1 x 10^{-12}
Optical transmitter (at output connector)	
Transmitter type	Laser
Center wavelength	760 to 870 nm
Maximum spectral width (RMS)	4 nm
Mean launch power	–5 to –10 dBm
Allowable extinction ratio	8 to 20 dB
Optical 10 to 90% transition times	≤ 300 ps
RIN (max)	–116 dB/Hz
Optical input to optical receiver	
Received optical power	– 16 dBm
Allowable extinction ratio	8 to 20 dB
Receiver return loss	≥ 40 dB
Discrete connector return loss	≥ 30 dB
Optical 10 to 90% transition time	≤ 360 ps
Optical path	
Optical fiber core diameter	50 or 62.5 µm
Minimum bandwidth at 780 nm:	
62.5 µm optical fiber	160 MHz · km
50 µm optical fiber	400 MHz · km
Mean fiber plant attenuation (DC)	0 to 4.0 dB
Discrete connector return loss	≥ 30 dB
Recommended connector	Duplex SC
Optional connectors	FC/PC or ST

Annex A
(informative)

Implementation suggestions

A.1 Example SUBMUX circuit

Figure A.1 shows a block diagram of an example SUBMUX circuit used to generate the M0 and M1 signals. The pulse width control circuits guarantee that the three adjacent CONNECT and READY bits are identical, and that only legal transitions on these signals are transmitted. A divide by 32 (0.8 MHz) signal from the 25 MHz divider circuit is used for the alternating 1/0 OH8 framing signal.

A.2 Example SUBDEMUX circuit

Figure A.2 shows a block diagram of an example SUBDEMUX circuit used to decode the received M0 and M1 signals. The Sync Control and Compare circuits are used to detect the alternating 1/0 pattern on OH8, thereby properly framing the Overhead bits. The circuitry performs a majority vote on the three adjacent bits to produce a CONNECT or READY signal which is immune to single bit errors. Before delivery to the local HIPPI-PH Source port, the CONNECT and READY signals should be stretched to at least 4 HIPPI-PH CLOCK periods to conform to ANSI X3.183, HIPPI-PH, subclause 7.7.

A.3 TLI and RLI availability

Hewlett-Packard part number HDMP-1012 is an example of a suitable TLI, and part number HDMP-1014 is an example of a suitable RLI and Link Control. This information is given for the convenience of the users of this standard and does not constitute an endorsement by ANSI, or other publisher of this standard, of these products.

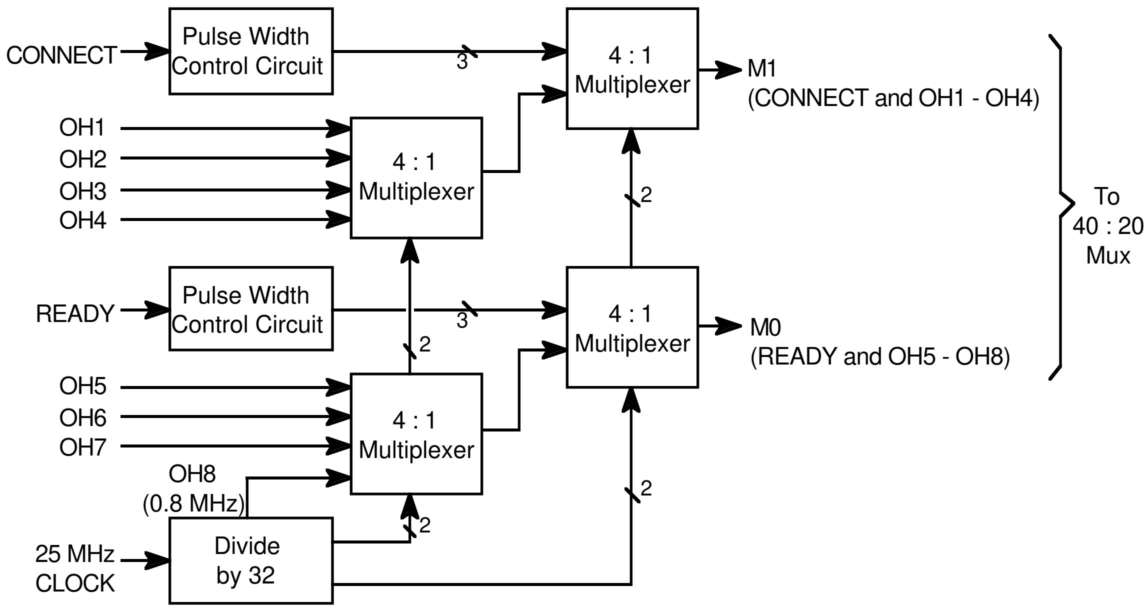

Figure A.1 – SUBMUX block diagram

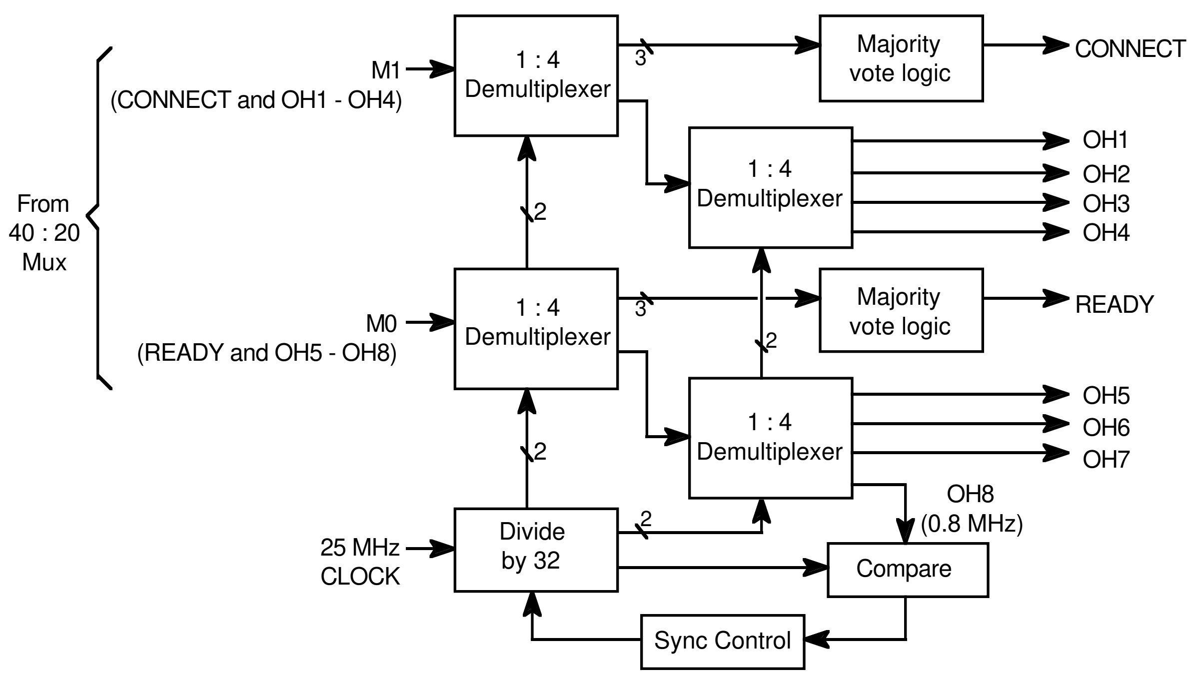

Figure A.2 – SUBDEMUX block diagram

Annex B
(informative)

Additional optical information

B.1 Eye measurements with an oscilloscope

The eye diagram parameters should be directly measured from the display of an oscilloscope triggered off of the source node's serial transmit bit clock. An oscilloscope bandwidth of at least 10 GHz should be used. The scope should be placed in infinite persistence mode and a total of approximately 20 million samples accumulated. This would require 5 to 10 minutes on typical sampling oscilloscopes. All eyes should be measured while the link is transmitting random data.

The optical receiver used to measure these eyes should have a sensitivity of better than –25 dBm at a bit error rate of 10^{-12} and a linear frequency response bandwidth of at least 5 GHz.

The eye measurements should be performed with a $2^{23}–1$ bit Pseudo-Random Bit Sequence. This sequence can be used directly, or can be encoded in the method presented in this document. Encoding can be accomplished by converting the $2^{23}–1$ PRBS serial sequence to a sequence of 32 bit words, plus 4 parity bits, and then inputting them to the HIPPI-Serial inputs as normal HIPPI input data.

B.2 Optical power

The optical power at the fiber connectors should be measured using a calibrated power meter with Fill Frame 0 being transmitted. This corresponds to a 50 MHz square wave test signal.

B.3 Optical spectrum

The center wavelength and spectral width of the transmitted optical signal should be measured using an optical spectrum analyzer. The patch cable used to couple the light from the fiber connector to the analyzer should be short to minimize spectral filtering by the patch cable. A $2^{23}–1$ PRBS should be used as the test pattern for testing the optical spectrum.

B.4 Eye safety

The maximum coupled power limits within this specification comply with the present IEC-825 standard for Class 1 eye safety.

B.5 Loss budget examples

Example loss budgets are given for typical configurations, and the basis for the losses are included.

B.5.1 Typical connector losses

For the loss budget examples, typical specifications for single-mode connectors are assumed to be:

Mean connector loss	≤ 0.25 dB
Standard deviation of connector loss	0.1 dB
Minimum optical return loss	30 dB

It is recommended that in a 10 km single-mode link no more than eight connectors be used between the optical transmitter and optical receiver .

Typical specifications for multimode connectors are:

Mean connector loss	≤ 0.11 dB
Standard deviation of connector loss	0.15 dB
Minimum optical return loss	30 dB

It is recommended that in a multimode link no more than eight connectors be used between the optical transmitter and optical receiver .

B.5.2 Splices losses

For the loss budget examples, the following is offered as the basis for the splice losses. It is assumed that a cable splice will be located at each end of the optical fiber plant and that there will be one splice per kilometer of cable. Two splices are assumed to be required for future optical fiber plant maintenance. The total number of splices in a system will then be:

Number of splices = 4 + (link length in km)

The characteristic of the system single-mode splices are assumed to be:

Mean splice loss	≤ 0.15 dB
Standard deviation of splice loss	0.1 dB

The characteristic of the system multimode splices are assumed to be:

Mean splice loss	≤ 0.08 dB
Standard deviation of splice loss	0.05 dB

The maximum number of splices in a multimode link is six.

B.5.3 Single mode loss budget example

+	Minimum laser launch power	– 9 dBm
–	Mean Plant Attenuation (DC) for 10 km system	– 9 dB
–	Three standard deviations of system loss: $3\sqrt{N\sigma^2}$ where N is the number of connectors/splices	– 1.4 dB
–	Optical receiver sensitivity	– 22 dBm
=	Minimum unallocated optical power margin	+ 2.6 dB

B.5.4 62.5 μm loss budget example

+	Minimum laser launch power	– 10 dBm
–	Maximum optical fiber loss	– 1.4 dB
–	Mean connector loss (8 each)	– 0.9 dB
–	Mean splice loss (6 each)	– 0.5 dB
–	3σ loss	– 1.4 dB
–	Optical receiver sensitivity	– 16 dBm
=	Minimum unallocated optical power margin	+ 1.8 dB

B.5.5 50 μm loss budget example

+	Minimum laser launch power	– 10 dBm
–	Maximum optical fiber loss	– 1.8 dB
–	Mean connector loss (8 each)	– 0.9 dB
–	Mean splice loss (6 each)	– 0.5 dB
–	3σ loss	– 1.4 dB
–	Optical receiver sensitivity	– 16 dBm
=	Minimum unallocated optical power margin	+ 1.4 dB

B.5.6 Multimode with 1300 nm laser loss budget

For the case of 1300 nm lasers and multimode optical fiber, the link is dispersion limited to 1 km and loss is a secondary consideration.

Annex C
(informative)

HIPPI-PH signal relationships

C.1 REQUEST, PACKET, and BURST

The HIPPI-PH signalling protocol specifies only four legal states of the REQUEST, PACKET, and BURST signals:

– The IDLE state is defined as REQUEST, PACKET, and BURST, all deasserted.

– The REQUEST state is when only REQUEST is asserted. This occurs when the Source is trying to make a connection.

– The PACKET state corresponds to both REQUEST and PACKET asserted, and BURST deasserted. This signifies the beginning of a packet, or the gap between successive BURST states.

– The BURST state is when REQUEST, PACKET, and BURST are all asserted. This occurs when the link is transmitting a burst of data.

All other combinations of the REQUEST, PACKET and BURST signals are defined as illegal in HIPPI-PH and are assigned to IDLE. Thus a HIPPI Source sequence error will cause the REQUEST line to be deasserted, and the connection will have to be reestablished at the HIPPI level. Note that this error does not cause the links to be reset.

C.2 Control signals during errors

When Frame Errors, i.e., not Data Frames, are detected, the HIPPI-PH REQUEST, PACKET, BURST, CONNECT, and READY control signals to the HIPPI-PH port are maintained at their previous values.

In other words, the control signals should not change from what they were in the previous Data Frame. This action is important because on a Frame Error the control signals may be inverted or scrambled. It is undesirable for the HIPPI port to receive scrambled control signals.

Holding the HIPPI-PH control signals to their previous value on Frame Errors is quite robust. In general these control signals switch relatively infrequently, so they would naturally have their previous value at least 75% of the time. In addition, holding the control signals constant and forcing a parity error in the data to the HIPPI port will result in no error unless data was being transferred, or an error that the HIPPI port may detect as a sequence error.

The following cases show what will occur if a Frame Error is received when the HIPPI connection is in various states. In each case, REQUEST, PACKET, BURST, CONNECT, and READY are held in the state described. The issue is how the HIPPI-PH port will react, and what effect the parity error forced into the data will have. These descriptions refer to operations defined in ANSI X3.183, HIPPI-PH.

C.2.1 Case 1

No connection - REQUEST and CONNECT deasserted –

The HIPPI-PH Destination should not be affected by the occurrence of parity errors since there is no active connection.

C.2.2 Case 2

Connection in process - REQUEST asserted, CONNECT deasserted –

A parity error will be forced in the I-Field, but the Destination will only act on it if it occurs when the Destination is sampling the I-Field. Normally, the I-Field is read when REQUEST goes true. In that case the I-Field will be valid, as REQUEST can only transition on a Data Frame. In any case, if a parity error is detected in the I-Field, the I-Field should be sampled again, or the connection refused.

C.2.3 Case 3

Connection complete, no packet in process - REQUEST and CONNECT asserted, PACKET deasserted –

The HIPPI-PH Destination should not be affected by the occurrence of parity errors since no data is being transferred.

C.2.4 Case 4

Connection complete, packet in process, no data moving - REQUEST, CONNECT and PACKET asserted, BURST deasserted –

The HIPPI-PH Destination should not be affected by the occurrence of parity errors since no data is being transferred.

C.2.5 Case 5

Starting a burst - REQUEST, CONNECT, and PACKET asserted, BURST transitions to asserted.

Since BURST will be held low, the burst will be shortened by one word. A bad LLRC should result. The data parity error that was forced will probably be ignored by the Destination HIPPI.

C.2.6 Case 6

Connection complete, passing data - REQUEST, CONNECT, PACKET, and BURST asserted.

A data parity error will be detected by the Destination HIPPI and any re-transmission will need to be requested by an upper-layer protocol.

C.2.7 Case 7

Connection complete, passing LLRC - REQUEST, CONNECT, and PACKET asserted, BURST transitions to deasserted.

The BURST signal will be held asserted, stretching the burst by one word, and a parity error will be forced into the data. If the next frame is a Data Frame, then the word following the true LLRC will be interpreted as the LLRC. This will almost certainly be in error. The HIPPI-PH Destination will see both the data parity error and a bad LLRC.

C.2.8 Case 8

Inter-packet gap - REQUEST and PACKET transition from true to false.

PACKET is required to be false at the destination for only one HIPPI clock cycle. Therefore, for the case of packets being transmitted at the maximum rate, it is possible to concatenate two packets, forming a single packet. This is an error that should be caught by a higher-layer protocol. The forced parity error will be ignored. If the PACKET spacing is greater than one HIPPI clock cycle, the HIPPI-PH Destination should not be affected by the occurrence of parity errors since no data is being transferred.

C.2.9 Case 9

A Frame Error occurs on some other HIPPI control signal transition.

The HIPPI signal(s) will be displaced by one clock. In most cases this will not be a problem. Problems may be caught by the HIPPI-PH Destination checking for the timing relationships specified in ANSI X3.183, HIPPI-PH, subclause 7.9.

Annex D
(informative)

HIPPI-PH Extender

A HIPPI-Serial Extender is an external unit that has a ANSI X3.183, HIPPI-PH, compliant port on one side, and HIPPI-Serial compliant port on the other side. For example, in figure 1, the HIPPI-PH signals on the left side of the figure would connect to another HIPPI-PH port with a copper twisted-pair cable. The Overhead bits would remain within the HIPPI-Serial Extender and not connect to the HIPPI-PH ports. The serial data streams on the right side would connect to another HIPPI-Serial unit.

HIPPI-Serial Extenders provide a communication facility that extends the physical range of HIPPI ports beyond the 25 m limitation imposed by the twisted-pair copper cables. Other than extended range, the user should see no difference in operation when using HIPPI-Serial either as an external Extender or integrated into a HIPPI node.

D.1 HIPPI-PH signals

The HIPPI-PH signals in figure 1 should fully comply with X3.183, HIPPI-PH, including the mechanical and electrical specifications as well as the signalling protocol.

D.1.1 INTERCONNECT signals

The INTERCONNECT signals from the HIPPI node to a HIPPI-Serial Extender are not used for any control functions, but may drive status indicators. The INTERCONNECT signals from a HIPPI-Serial Extender to a HIPPI node should be statically driven with 220 Ω resistors to V_{EE} as defined in clause 8.2.2 of ANSI X3.183, HIPPI-PH.

D.1.2 Shaping CONNECT and READY signals

Since a clock signal does not accompany the CONNECT and READY signals, using the internal clock of a Serial-HIPPI implementation to strobe the CONNECT and READY signals may result in internal signals wider or narrower than expected due to sampling as the signals are changing. As specified in 6.5, the CONNECT and READY signals should be shaped to be a minimum of four HIPPI-PH CLOCK cycles wide.

D.1.3 Losing READY indications

If the HIPPI Destination has a faster CLOCK than the Serial-HIPPI implementation, and the Destination sends long sequences of minimum width READY signals, i.e., continuous back-to-back eight-CLOCK-period READY indications, then there is the possibility of losing one in 5000 READY indications. Lost READY indications should not occur unless both conditions are met, i.e., a pathological case. Clause 5.3.6 in ANSI X3.183, HIPPI-PH, describes the possibility of lost READY indications. HIPPI-PH, 5.3.6, does not require Sources to accept more than 63 READY indications, but Serial-HIPPI implementations that can accept up to 255 READY indications without loss are desirable. The onset of the first lost READY indication can be delayed through various means, including but not limited to:

– a design that tolerates receiving a few short READY indications before dropping an output READY indication, or;

– using a flag bit or special states to indicate that the forwarded READY indications are behind and need to catch up, when able, e.g., when receiving more than four contiguous CLOCK periods of READY asserted or READY deasserted, or;

– using a counter, counting up for each READY indication received, and counting down for each READY indication forwarded.

D.2 HIPPI-Serial Extender loopbacks

There are two desirable loopback modes for diagnosing a fault in a HIPPI-Serial Extender: local and remote. Figure D.1 illustrates both, with local loopback designated by LLB and remote loopback designated by RLB. These two modes of loopback allow the isolation of faults to the local end, the remote end, or the fiber optic cable, enhancing maintainability of the system.

D.2.1 Local loopback

The task of local loopback is to test the circuitry at the local end. The local loopback path should therefore include as much of the circuitry at the local end as possible. Ideally this would be implemented with an optical switch which would re-route the outgoing optical signal to the local optical receiver. However, a more economical approach is to re-route the serial electrical data stream from the output of the TLI to the input of the RLI. When a node is in local loopback, no data should be transmitted on the serial link.

D.2.2 Remote loopback

The task of remote loopback is to test the fiber optic cable between nodes. Therefore, the remote loopback path should contain only the cables, and as little of the remote node electronics as possible. Ideally this would be implemented by a switch that re-routes the received serial electrical signal directly to the serial optical transmitter.

An easy method to implement is to manually connect the remote HIPPI-Serial Extender's HIPPI-PH Source and Destination ports with a HIPPI cable. While this scheme does not offer the advantages of the direct RLI-TLI connection described above, it is the easiest to implement.

There is no need to be able to request that a local loopback test be performed at the remote node. If local loopback and remote loopback tests both pass, but there is still a high error rate on the link, the failure can be isolated to the remote circuitry by elimination. Note that under catastrophic failure a remote loopback command will fail, as the remote node will not even be able to receive the command. Remote loopback is, therefore, most useful when troubleshooting a high error rate that does not cause complete failure of the link.

When a node is requested to go into remote loopback (echo all data back), the signals delivered to the HIPPI-PH port should be set to zeroes. This will break all present connections, and prevent any connections from being established during remote loopback.

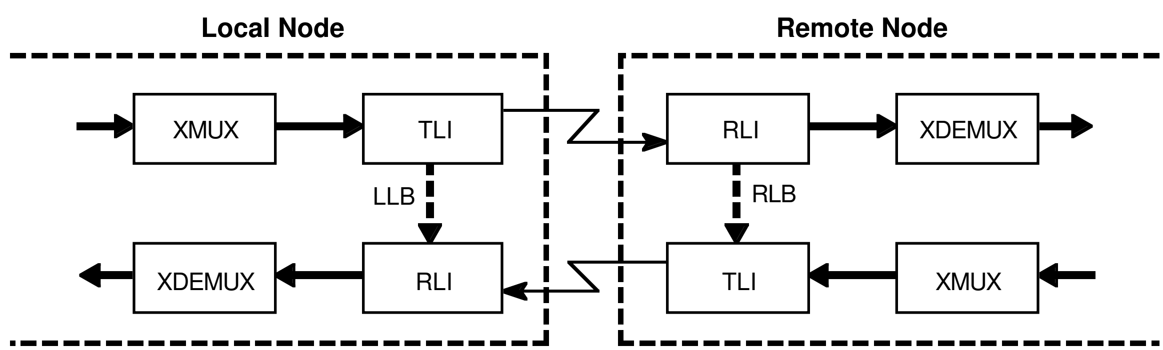

Figure D.1 – Remote and local loopback

D.3 HIPPI-Serial Extender front panel user interface

It is desirable to include operator controlled switches on a HIPPI-Serial Extender for:

– Reset: causes a complete restart of the link

– Disable 64-bit (1600 Mbit/s) mode: allows a 64-bit HIPPI-Serial to operate in a 32-bit (800 Mbit/s) mode

– Local loopback: connects the serial output of the TLI to the input of the RLI at the same node

– Remote loopback: requests the remote node to echo all data back to the local node

It is desirable to include operator indicators showing:

– the state of the TLI signals, as in 7.1 and 7.2;

– the type of frames, i.e., as in 6.2, being detected by the RLI;

– the state of the HIPPI control signals including INTERCONNECT, REQUEST, PACKET, BURST, and READY;

– local loopback, remote loopback (transmitting RL), or echoing data for the remote node (receiving RL) operation; and

– the status of the Parallel Parity Error (PP) and Serial Parity Error (SP) bits.

It is desirable to include connectors for transmit and receive of the Overhead bits OH2-OH7. The connector type is not specified.

Annex E
(informative)

Bibliography

The following references describe the 20b/24b coding used in HIPPI-Serial.

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[4] "DC-Free Code for Arbitrary Data Transmission", Doug Crandall, Steve Hessel, Tom Hornak, Rasmus Nordby, Kent Springer and Richard C. Walker, U.S. Patent Pending

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